



MS-7599 VER:1.1

CPU

AMD AM3 Socket 941

System Chipset

AMD RX780

ATI SB710/700/750

On Board Chip

FINTEK Super I/O -- F71889

LAN -- RTL8111DL

HD Codec --ALC888VC2

BIOS -- SPI ROM 8M

Main Memory

DDR III X 4 (Max 8GB)

Expansion Slots

PCI-E X 16 *1

PCI-E X 1 *2

PCI 2.2 Slot X 3

PWM

Controller--Intersil ISL6323 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

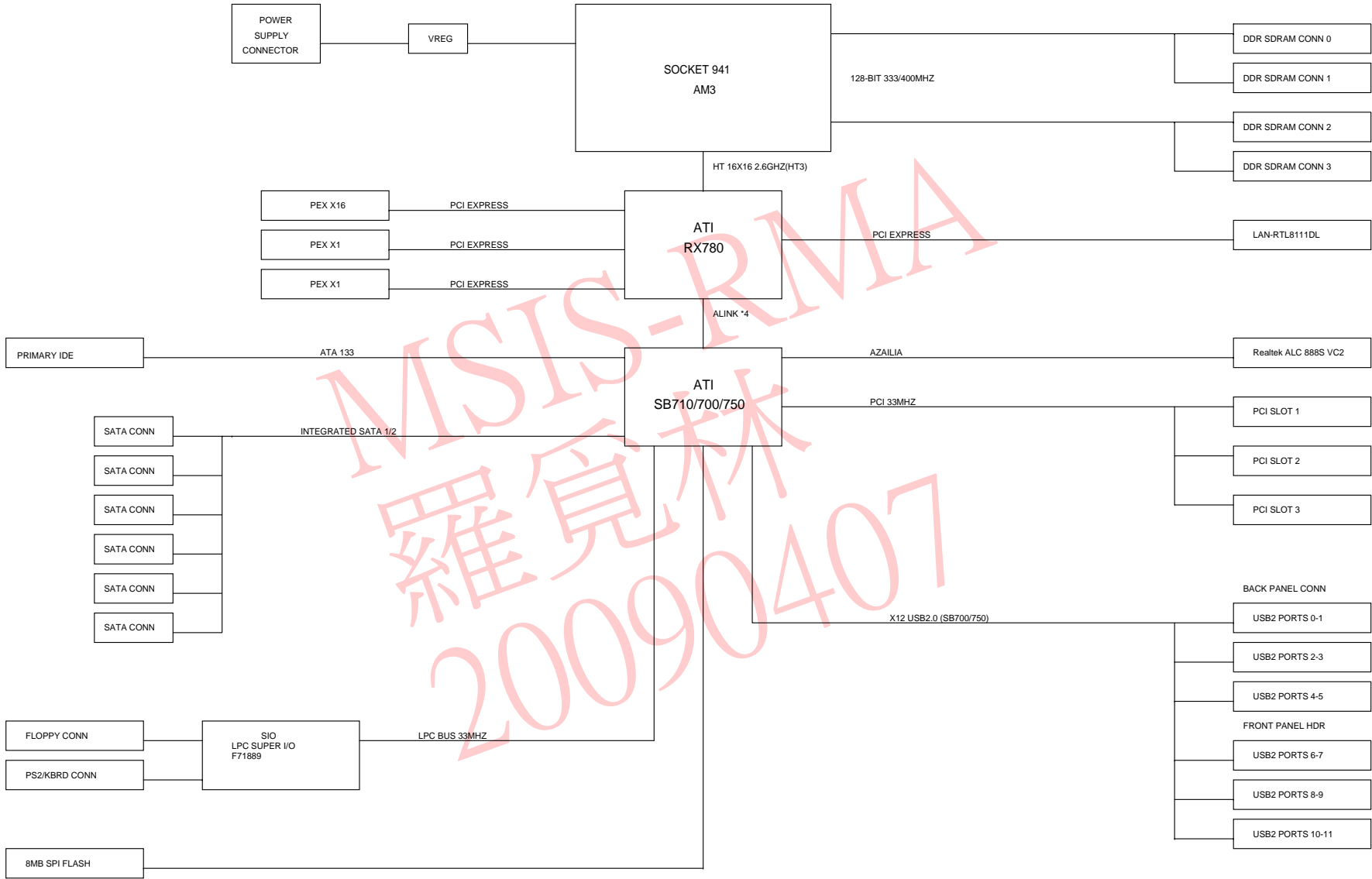
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Clock Generator

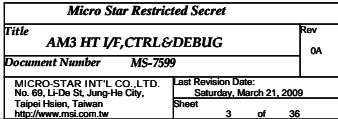
Controller--RTM880N-793

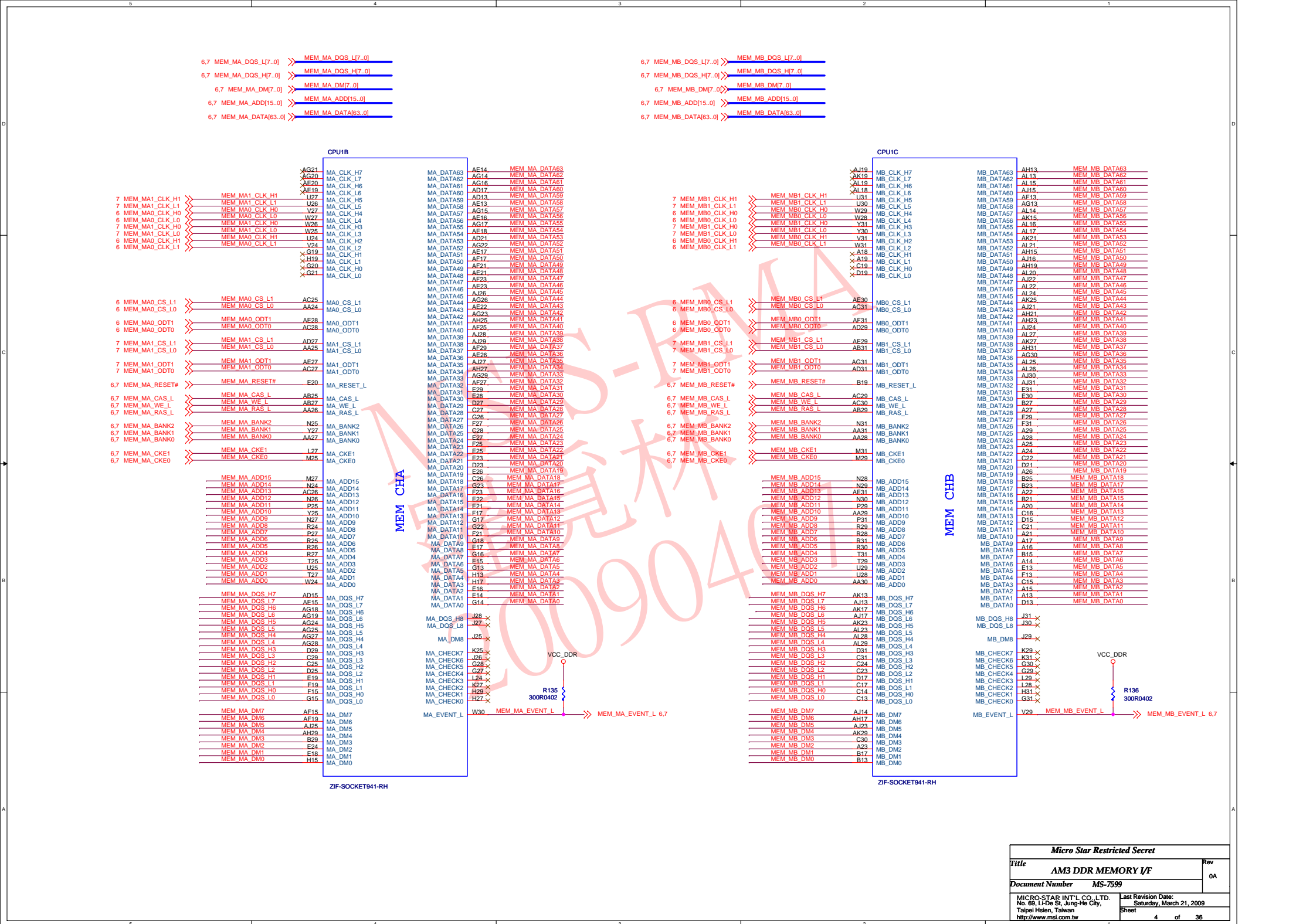
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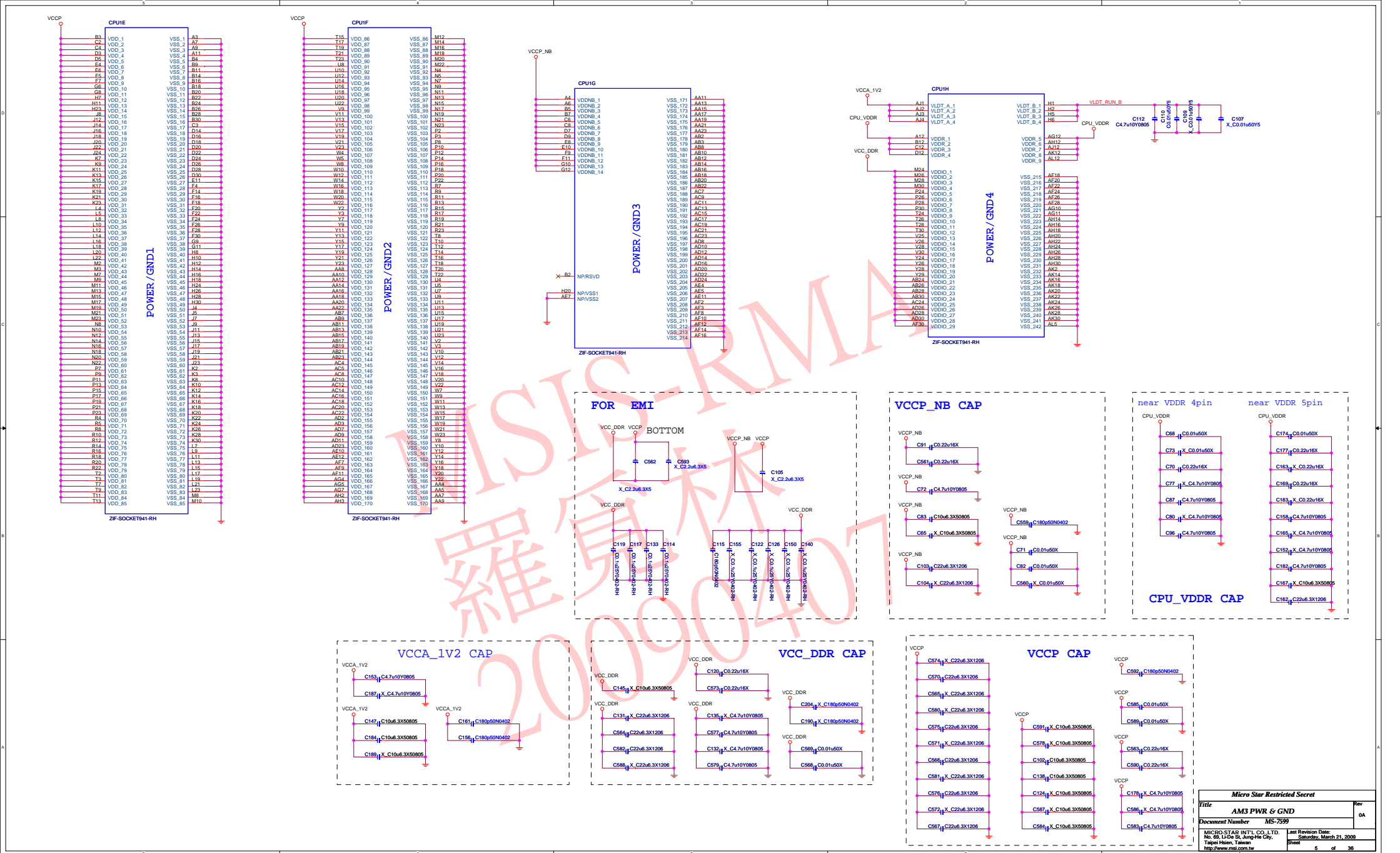
BLOCK DIAGRAM



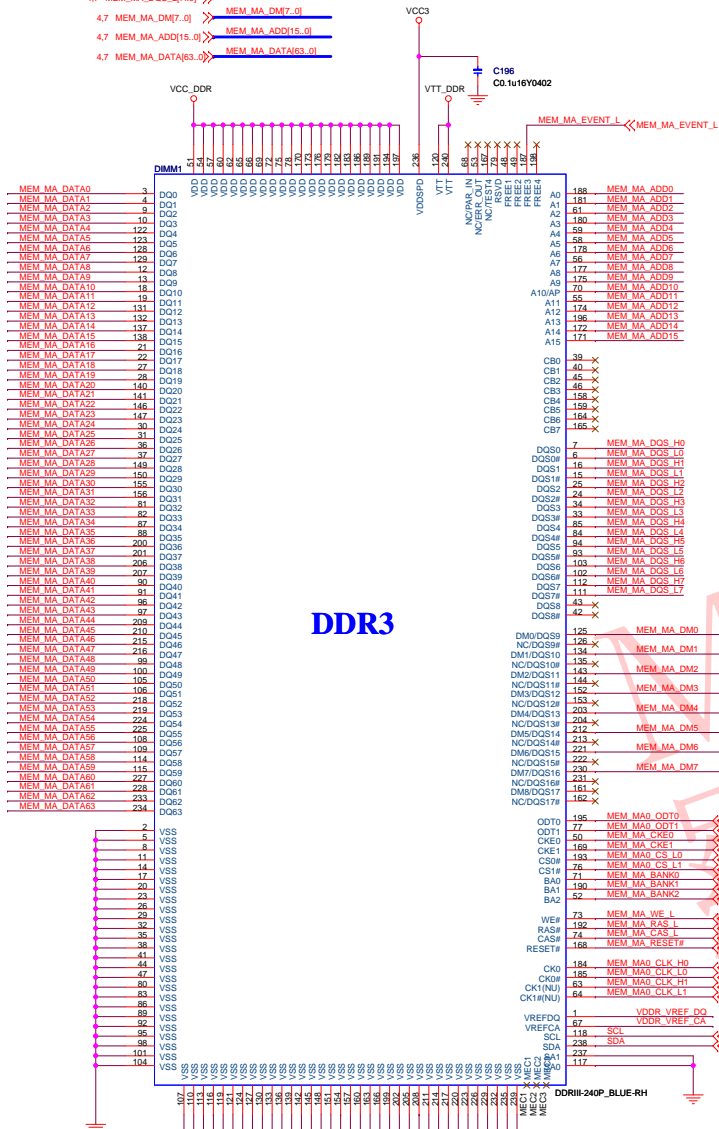
Micro Star Restricted Secret		
TitleBlock Diagram		Rev0A
Document NumberMS-7599		
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4.7 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
 4.7 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
 4.7 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
 4.7 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
 4.7 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]



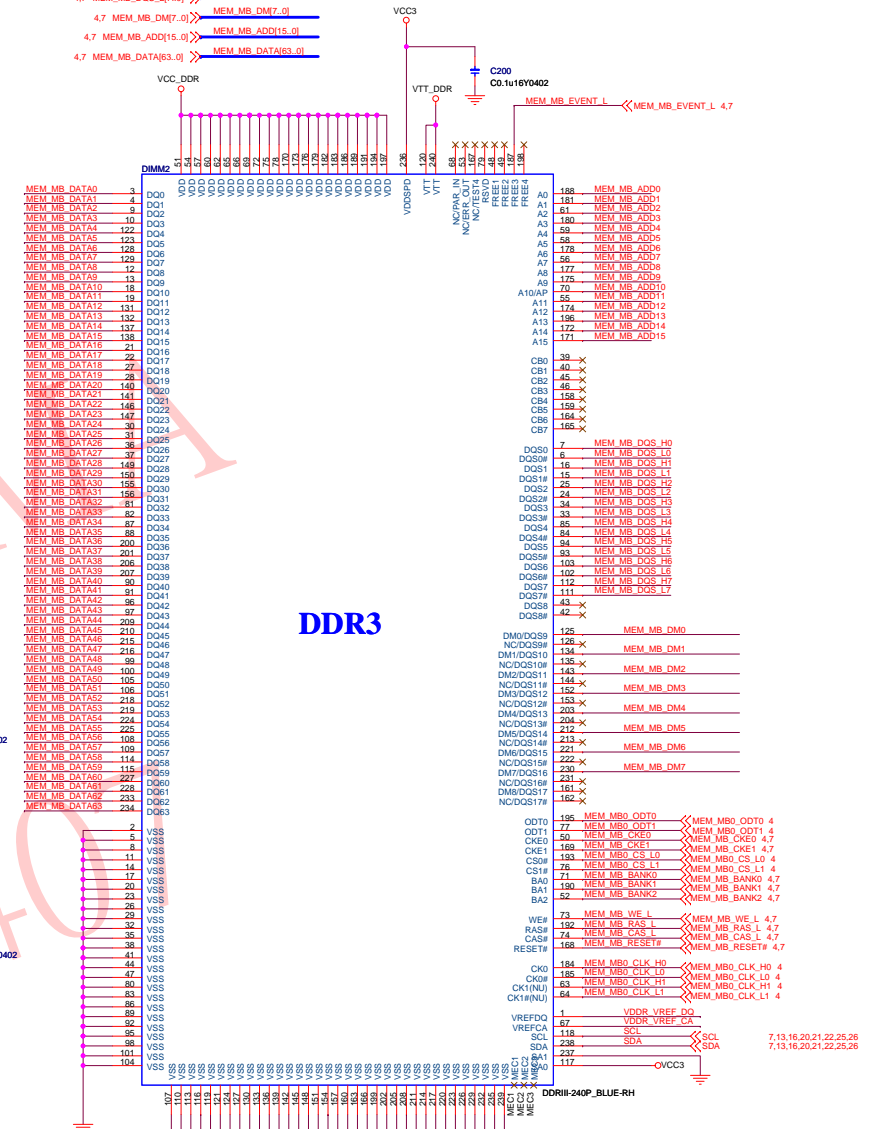
DDR3

ADDRESS A0

SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

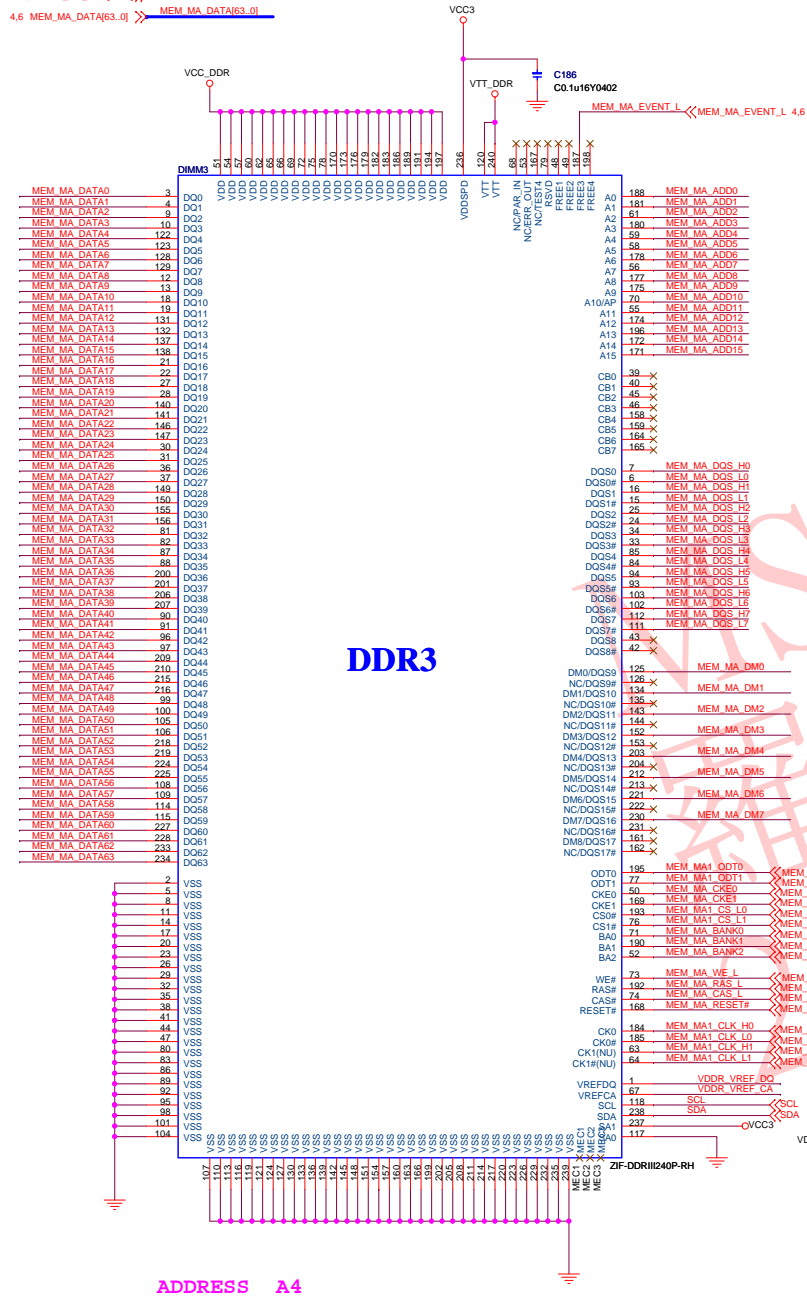
4.7 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
 4.7 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
 4.7 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
 4.7 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
 4.7 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



DDR3

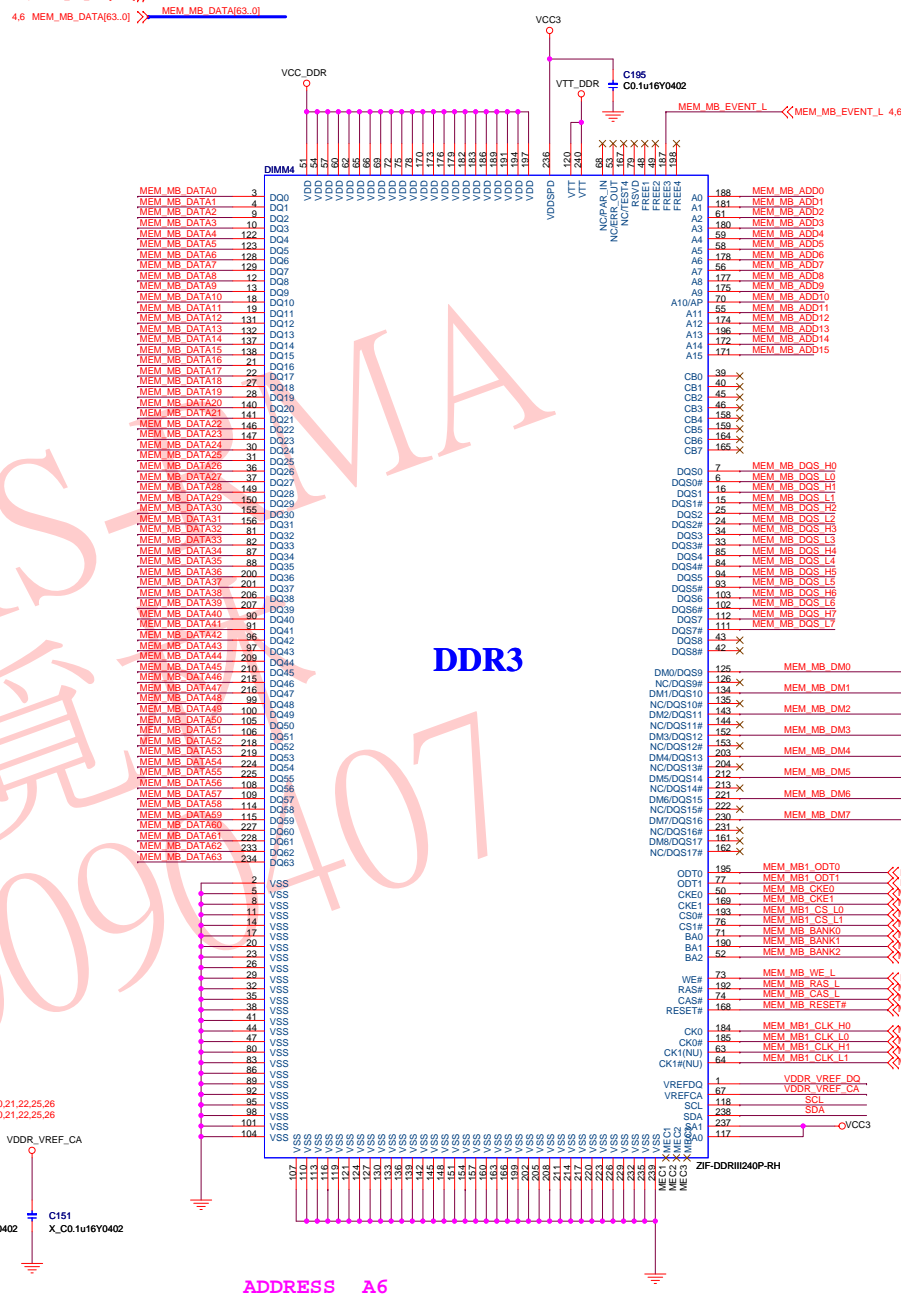
ADDRESS A2

4.6 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
4.6 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
4.6 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
4.6 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
4.6 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]



ADDRESS A4

4.6 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
4.6 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
4.6 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
4.6 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
4.6 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

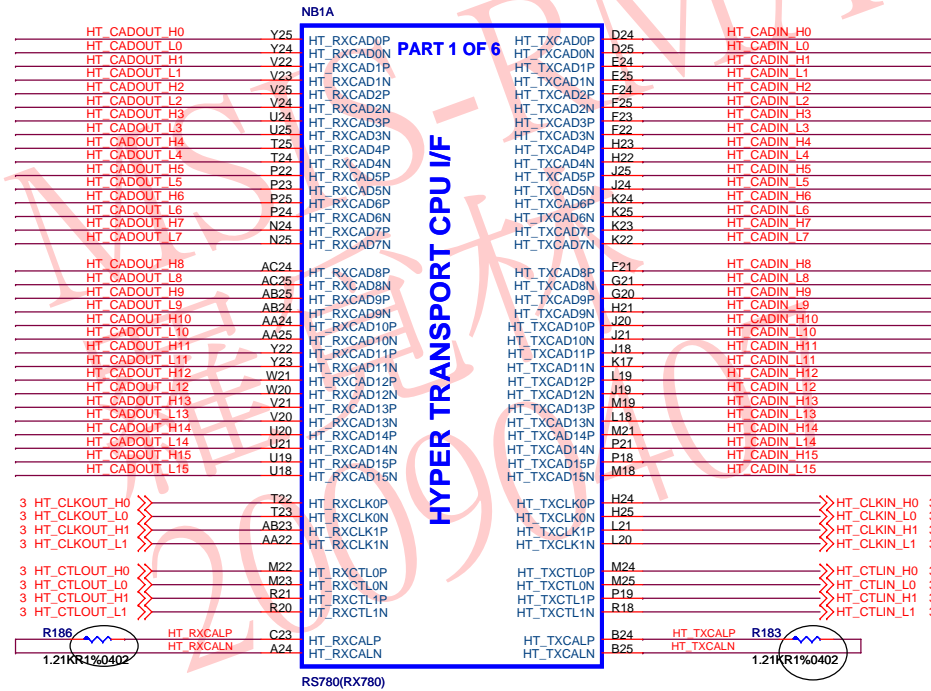


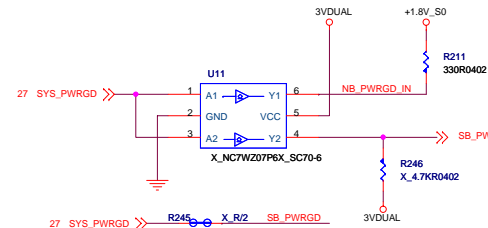
ADDRESS A6

3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

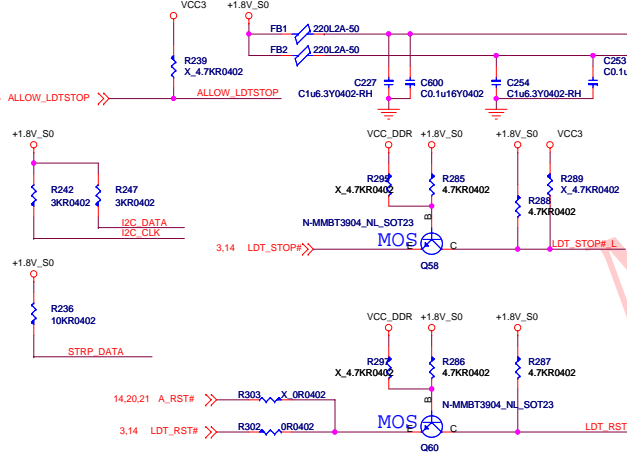
RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780/RS780
HT_RXCALP	49.9R (GND)	1.21K
HT_RXCALN	49.9R (VDDHT)	
HT_TXCALP	100R	1.21K
HT_TXCALN		





	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP_OUT(default)/IN	OD	OD	OD/3.3V IN
LDT_STOP#_IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb_IN	3.3V IN	1.8V IN	3.3V IN



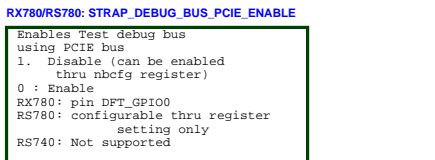
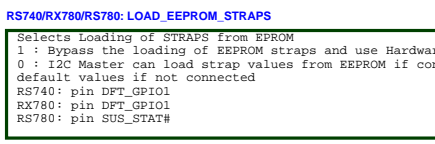
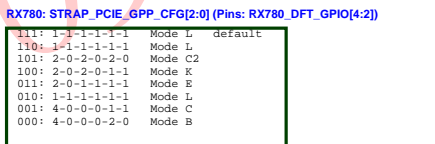
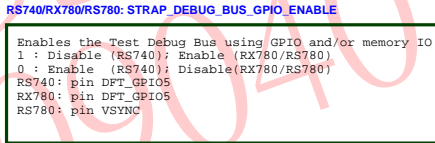
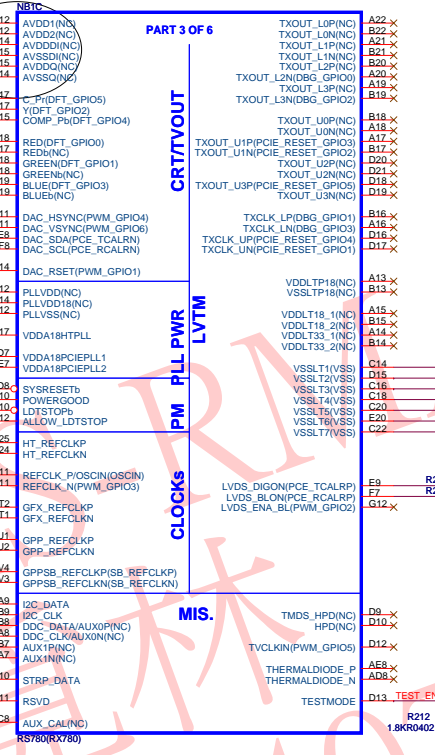
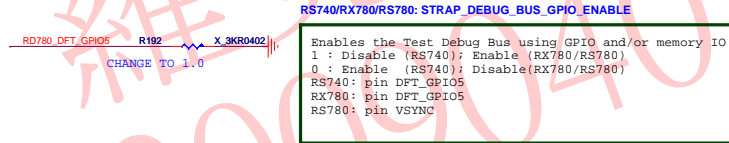
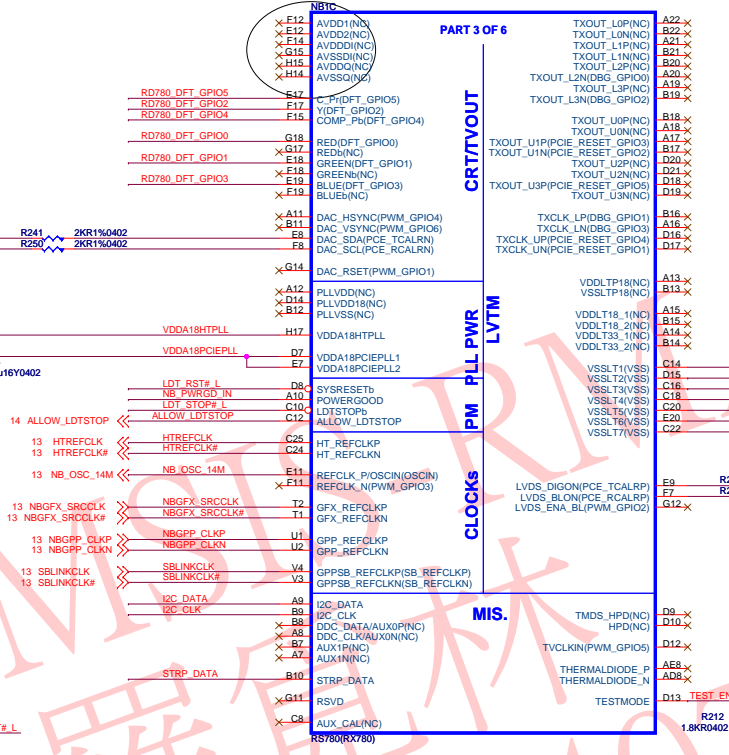
	RS780	RX780	SB700	CPU
LDT_STOP#	3.3V IN	VDD18/IN	OD	1.8V IN
LDT_RST#	SYSREST 3.3V IN	SYSREST VDD18/IN	OD	1.8V IN
ALLOW_STOP#	OD	OD/VDD18	3.3V IN	NA
POWERGOOD	VDD18/IN	VDD18/IN	NA	NA

* CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.



RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLO	LVDS_BLO
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

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Title	RD780/RX780-HT LINK I/F	Rev	0A
Document Number	MS-7599		
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NB1D		PAR 4 OF 6
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)
AA12	MEM_A4(NC)	MEM_DQ4(NC)
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)
AC14	MEM_A12(NC)	MEM_DQ12(NC)
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)
AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)
AD17	MEM_BA2(NC)	
	MEM_DQS0P/DVO_IDCKP(NC)	Y17
	MEM_DQS0N/DVO_IDCKN(NC)	W18
W12C	MEM_RASb(NC)	AD20
Y12C	MEM_CASb(NC)	AE21
AD18C	MEM_WEb(NC)	
AB13C	MEM_CSb(NC)	W17
AB18	MEM_CKE(NC)	AE19
Y14	MEM_ODT(NC)	
		IOPLLVD18(NC)
V15	MEM_CKP(NC)	AE23
W14	MEM_CKN(NC)	AE24
		IOPLLVD(NC)
AE12	MEM_COMPP(NC)	AD23
AD12	MEM_COMPN(NC)	AE18
		MEM_VREF(NC)

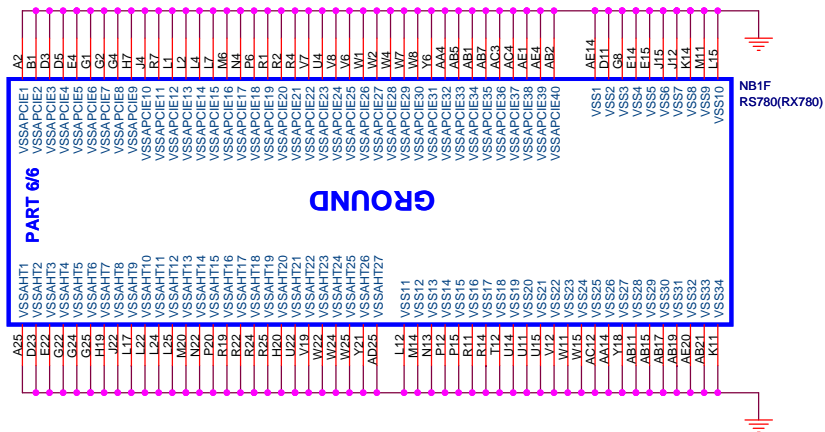
RS780(RX780)

Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

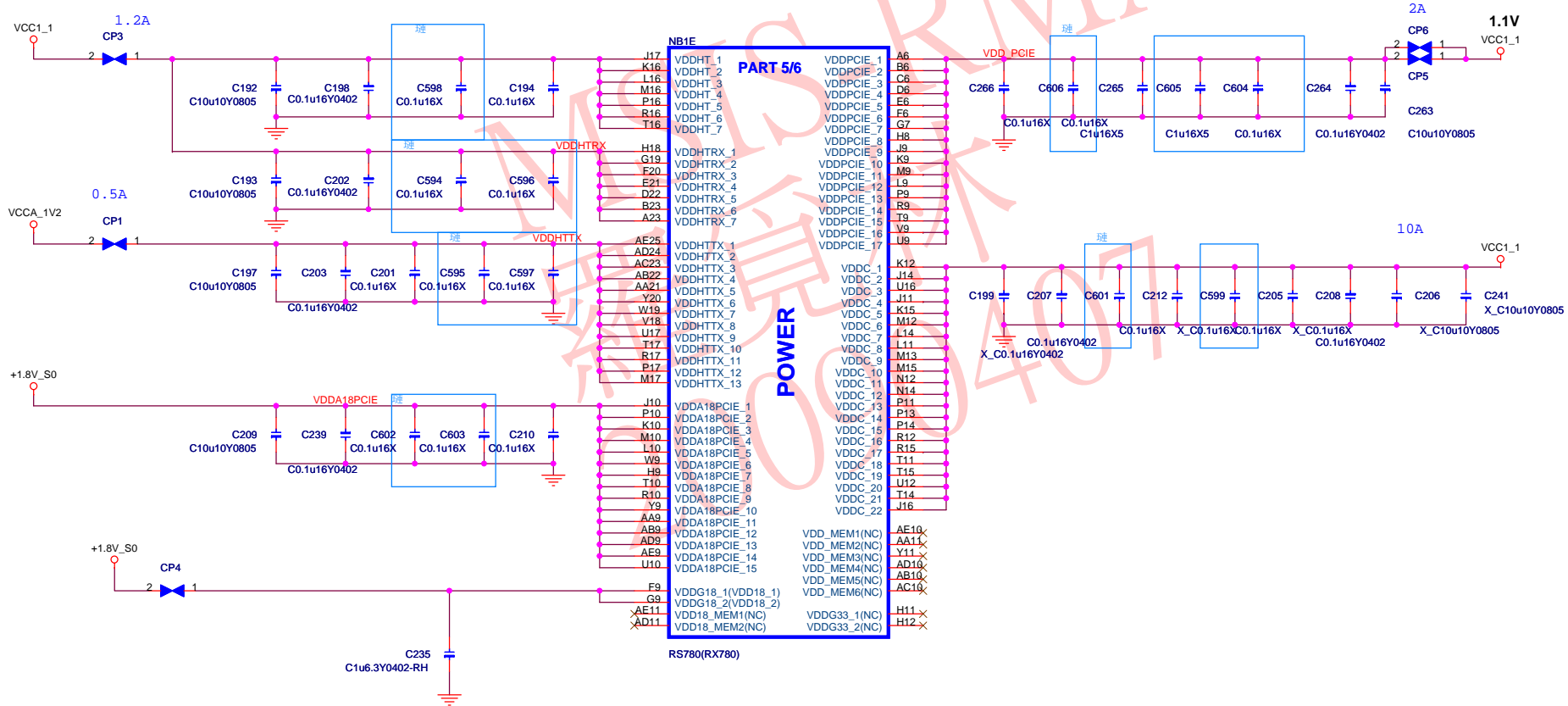
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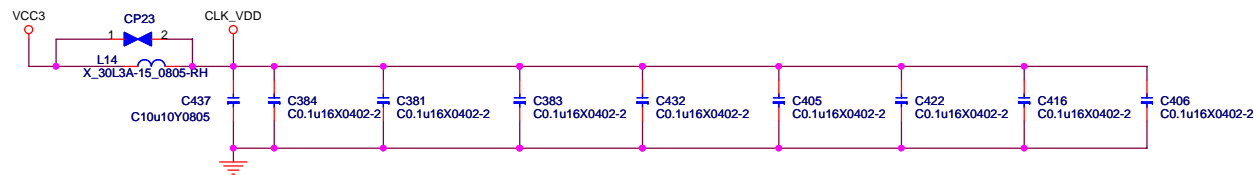
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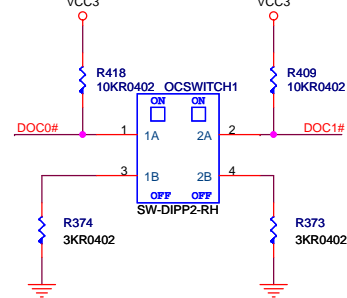
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC

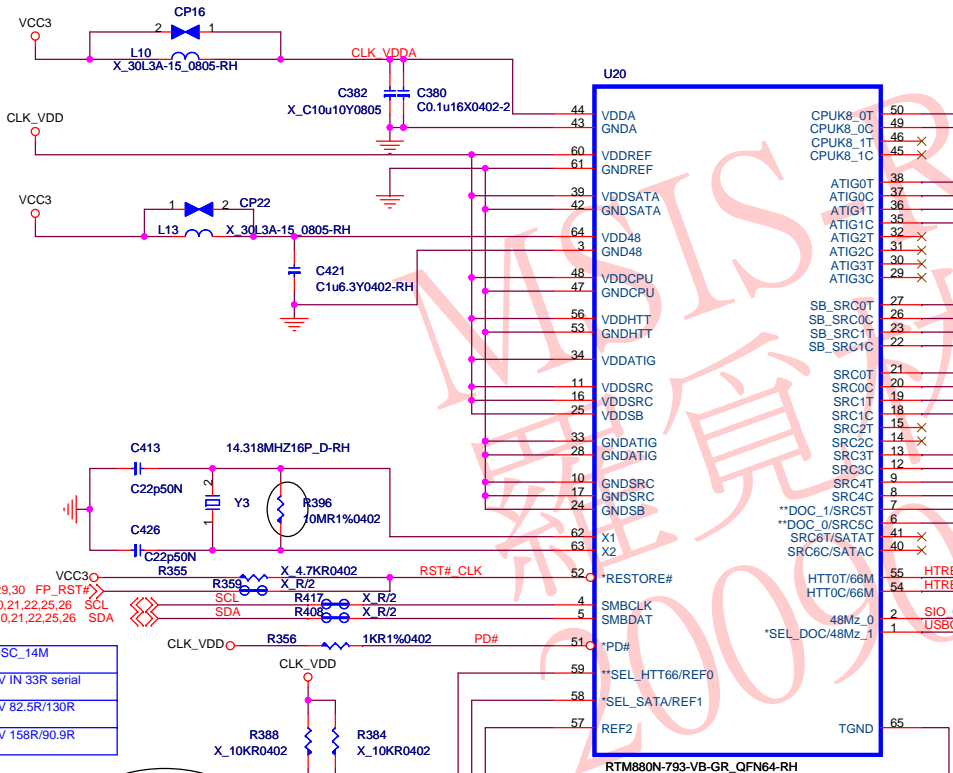




- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U41 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U41 POWER PIN



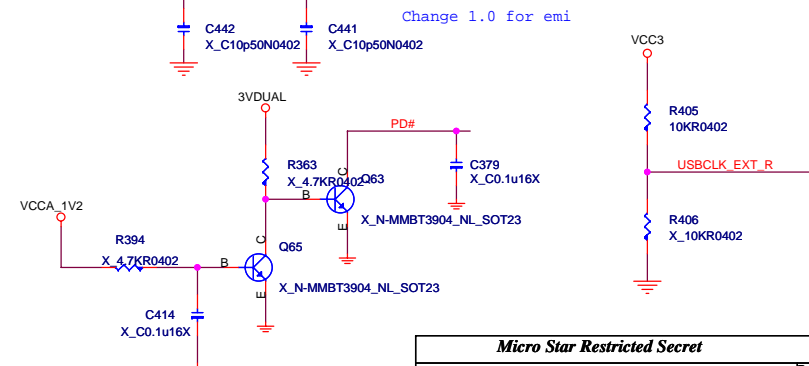
DOC1	DOC2	CPU Frequency
0	0	200MHz DEFAULT
0	1	250MHz,{CR07[7:5], CR08[7:0]}
1	0	300MHz,{CR14[2:0], CR13[7:0]}
1	1	350MHz,{CR1C[2:0], CR15[7:0]}



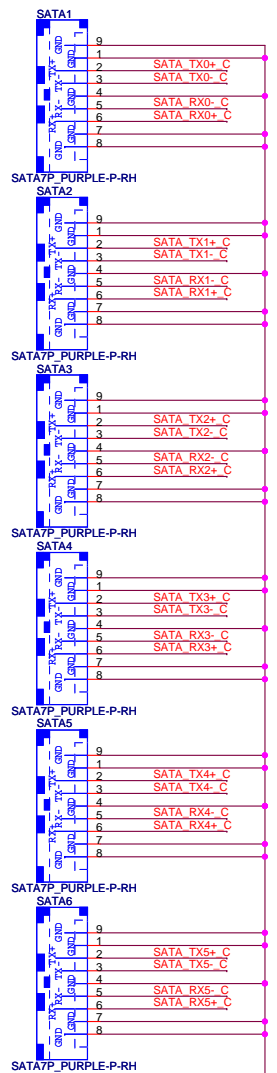
NB_OSC_14M	
RS740	3.3V IN 33R serial
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

SB_OSC_14M	
SB7XXA13	1.2V 110R
SB7XXA14	3.3V 33R

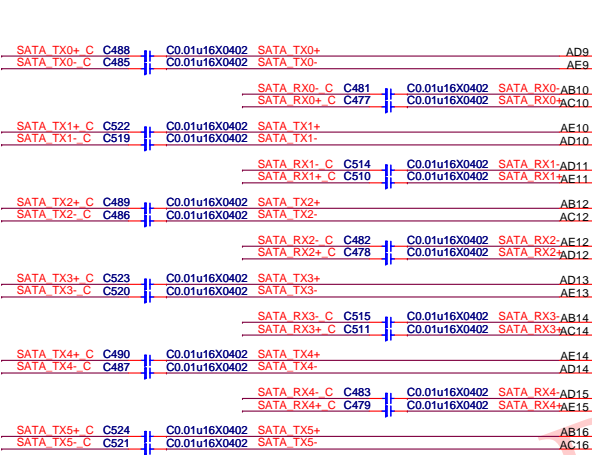
SEL_HTT66 : 'L' 100Mhz FOR 780
'H' 66Mhz FOR 740



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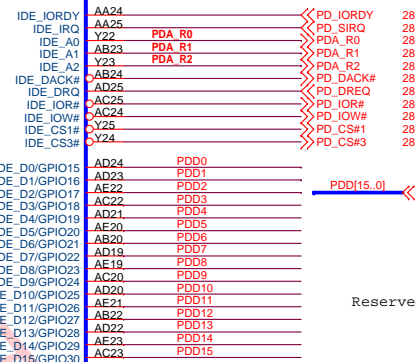
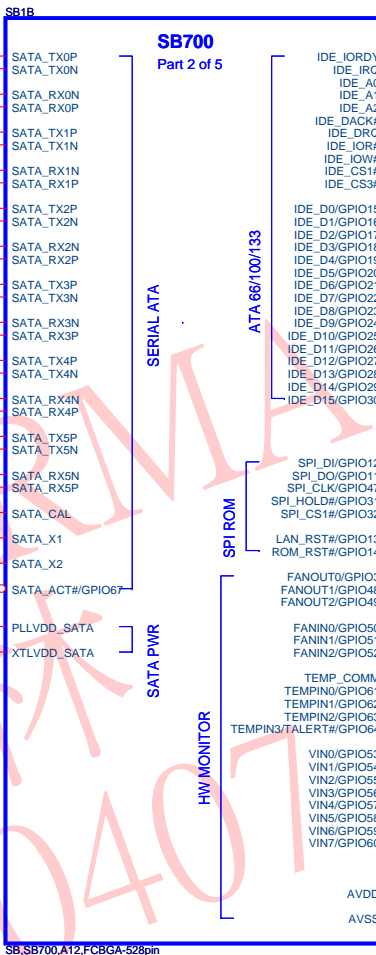
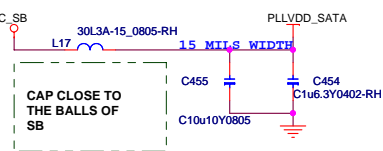
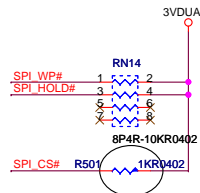
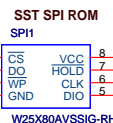
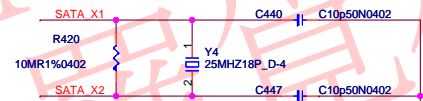


Impedance 90 Ohm, refer to AN_SB700AB2

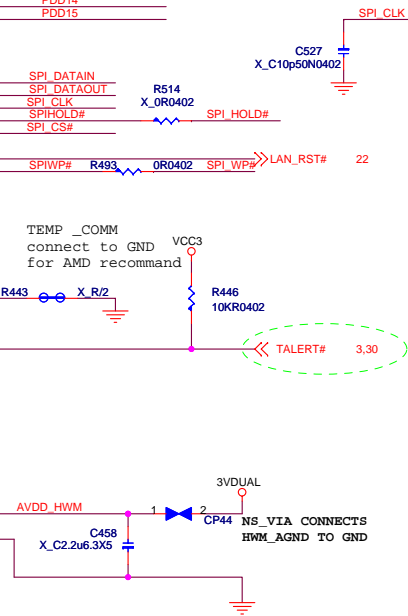


R272 IS 1K 1% FOR XTAL,
4.99K 1% FOR INTERNAL CLK

N5N-07M0231-H06



Reserved for EMI 0906

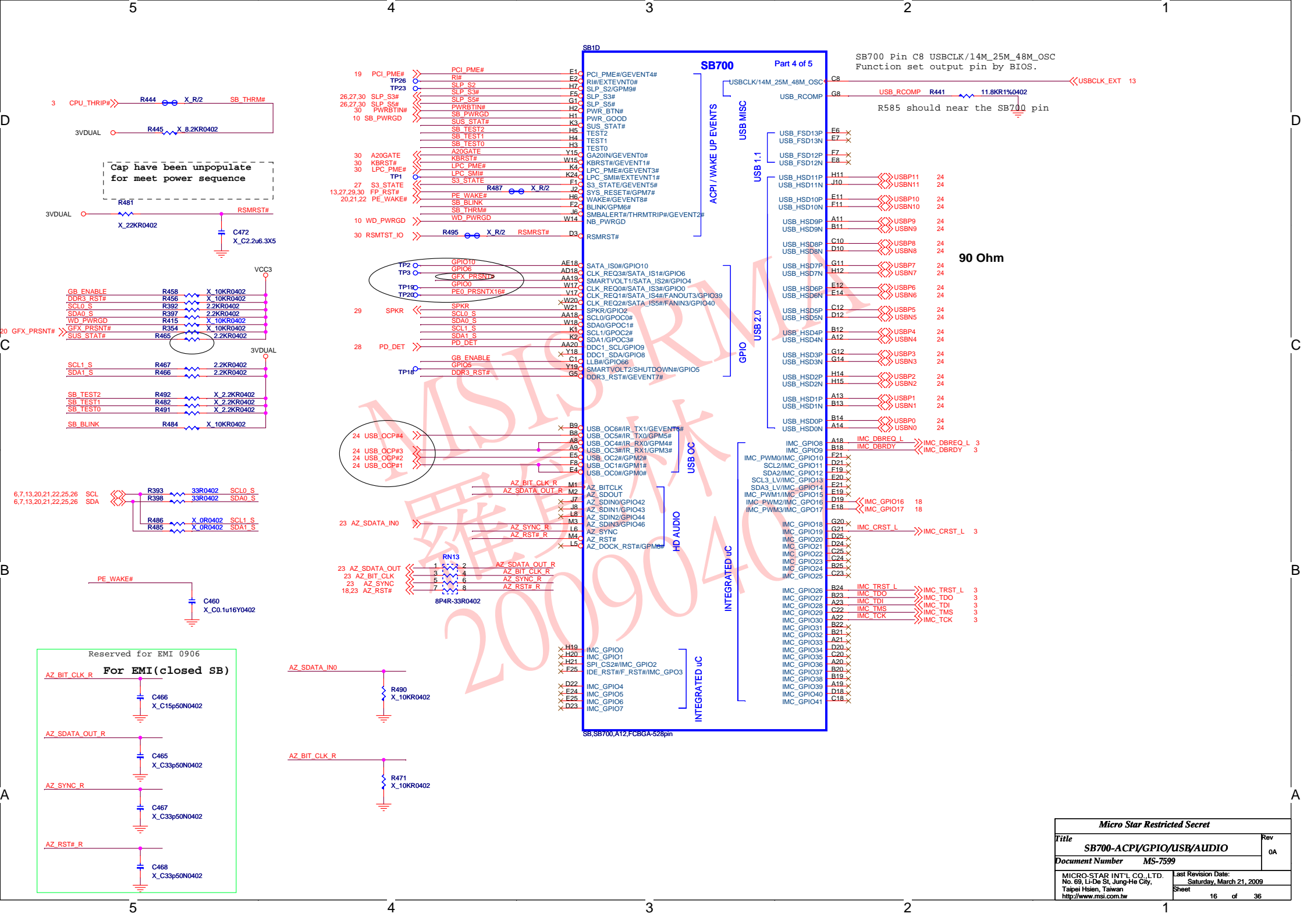


SPI FLASH MEMORY

SPI DEBUG PORT
Place close to SPI ROM

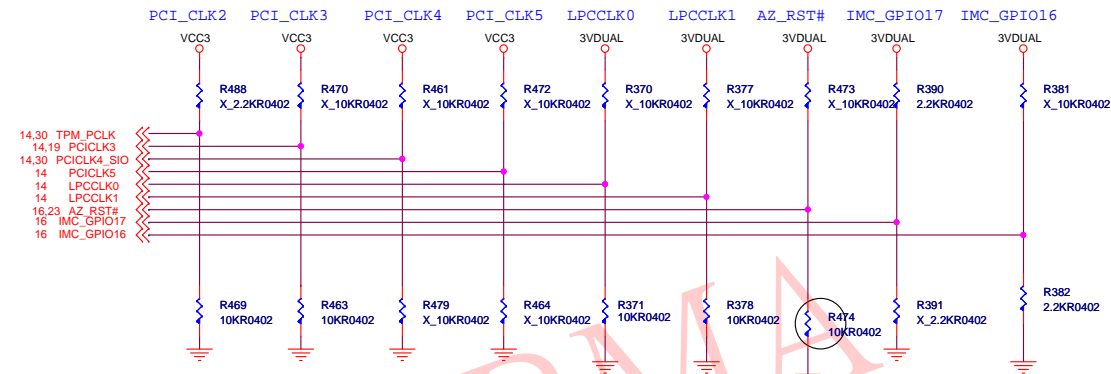
Part Number : N31-2051451-H06

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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



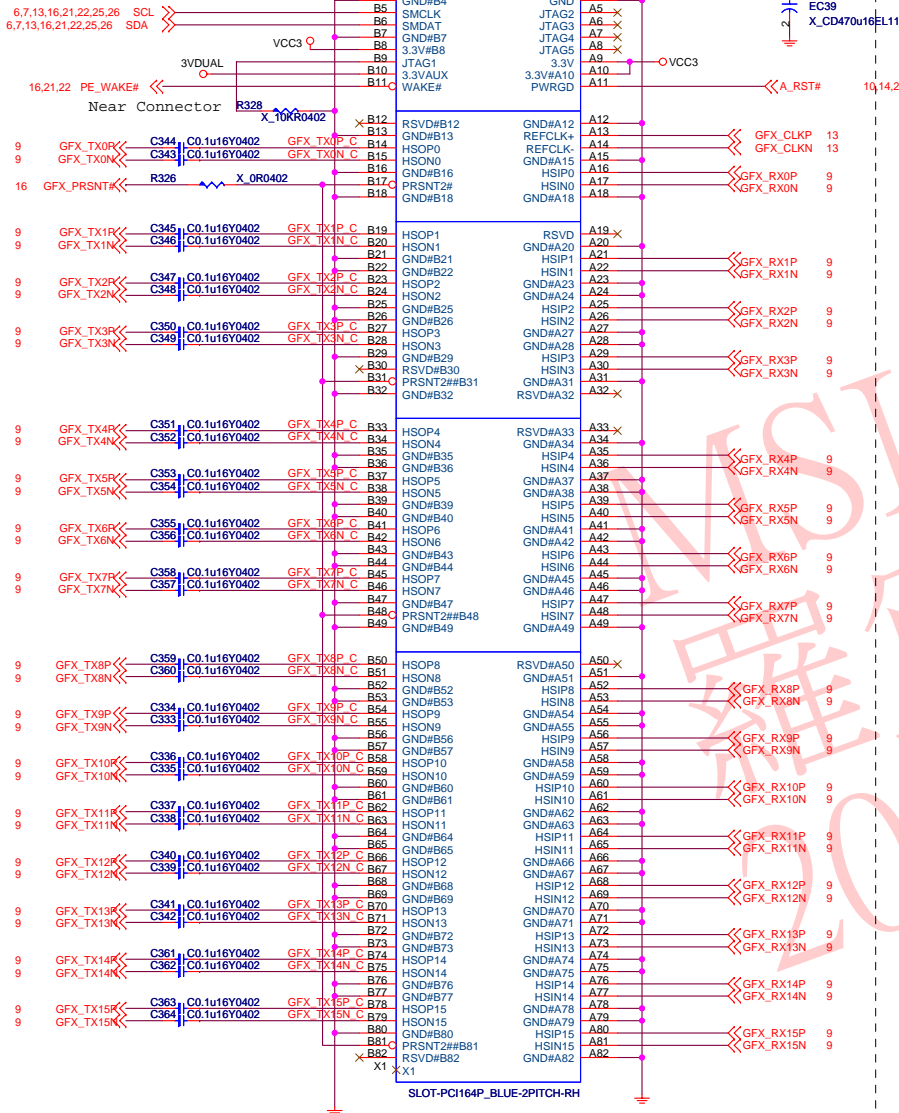
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM	DEFAULT

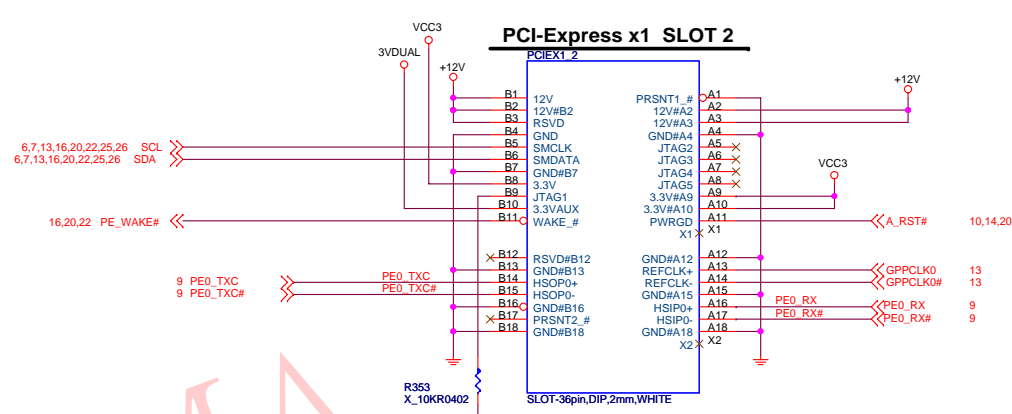
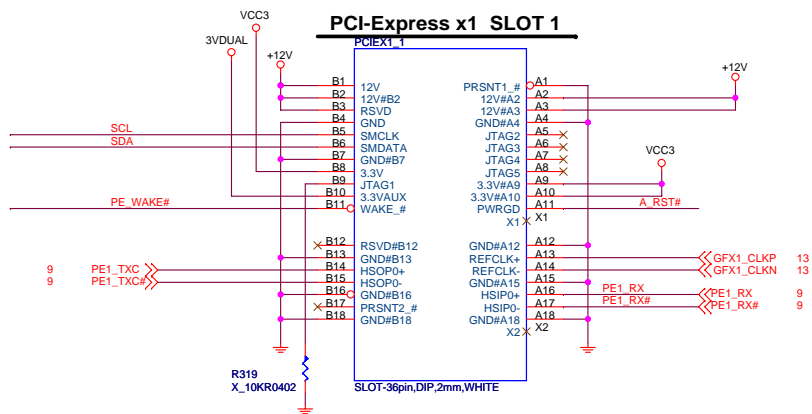
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

PCI EXPRESS 16

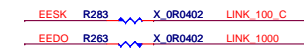




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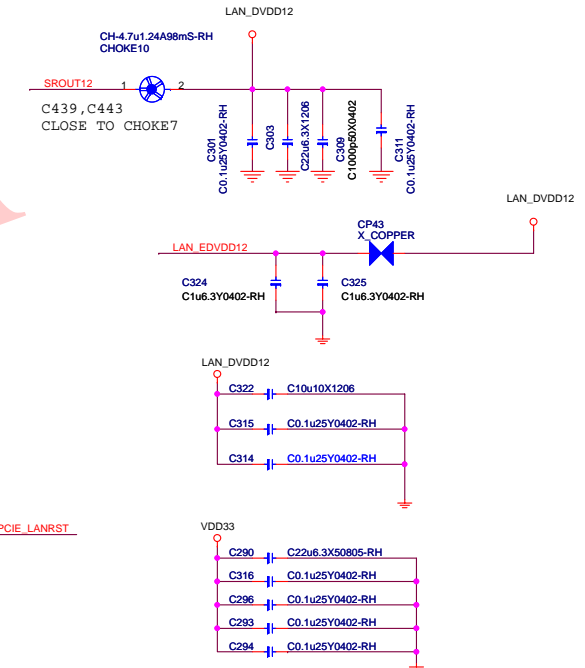
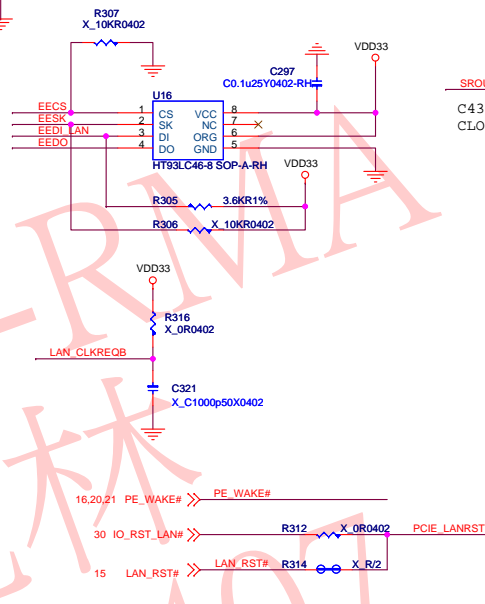
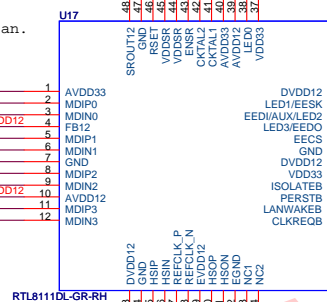
Title PCIE X1 Slot 1 , 2		Rev 0A
Document Number MS-7599		
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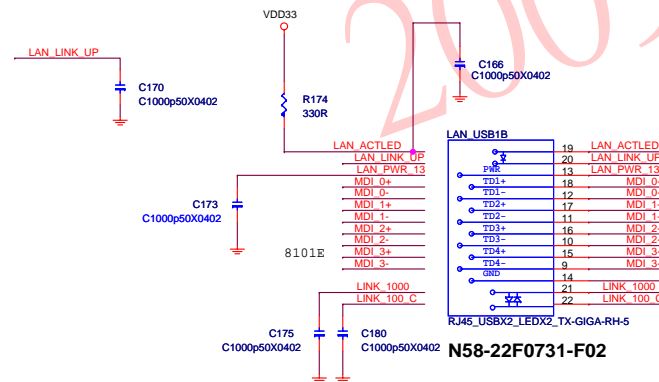
The schematic diagram illustrates the power supply section of the ADXL345 evaluation board. It features a 3V DUAL input connected to a voltage divider consisting of CP8 and X_COPPER. The output of this divider is connected to a decoupling network. This network includes a 365 ohm resistor (C365) in series with a 100nF capacitor (EC40) to ground. Following this, there is a 1uF capacitor (C307) in series with a 0.1uF capacitor (C330) to ground. The final output is labeled AVDD33. The schematic also shows connections to VDD33 and AVDD33 pins.

Diagram illustrating the connection of the NN-CMKT3904_SOT363-6-RH component. The component is connected to VDD33, EESK, EEDO, LINK_1000, and LINK_100. The component is labeled NN-CMKT3904_SOT363-6-RH.

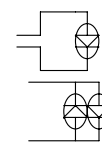
AVDD33	1	AVDD33	DVDD12	36	LAN_DVDD12
MDI_0+	2	MDIP0	LED1/EESK	35	EESK
MDI_0-	3	MDIP0	LED2/EED1	34	LED1_LAN
LAN_DVDD12	4	MDIN0	EED1/AUX/LED2	33	EED0
MDI_1+	5	MDIP1	LED3/EED0	32	EESK
MDI_1-	6	MDIP1	ECS	31	
MDI_2+	7	MDIN1	GND	30	LAN_DVDD12
MDI_2-	8	GND	DVDD33	29	DVDD33
MDI_3+	9	MDIP2	VDD33	28	ISOLATEB
LAN_DVDD12	10	MDIN2	ISOLATEB	27	PCIE_LANRST
MDI_4+	11	AVDD12	PERSTB	26	PER_WAKEB
MDI_4-	12	MDIP3	LANWAKEB	25	LAN_WKREB
MDI_5+	13	MDIP3	NC	24	NC
MDI_5-	14	MDIP3	NC	23	NC







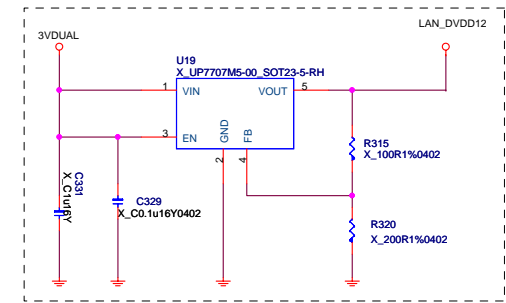
	RTL8111DL	
AVDD33	3.3V	
VDDSR	3.3V	
VDD33	3.3V	
EVDD12	1.2V	
DVDD12	1.2V	
AVDD12	1.2V	



Power consumption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

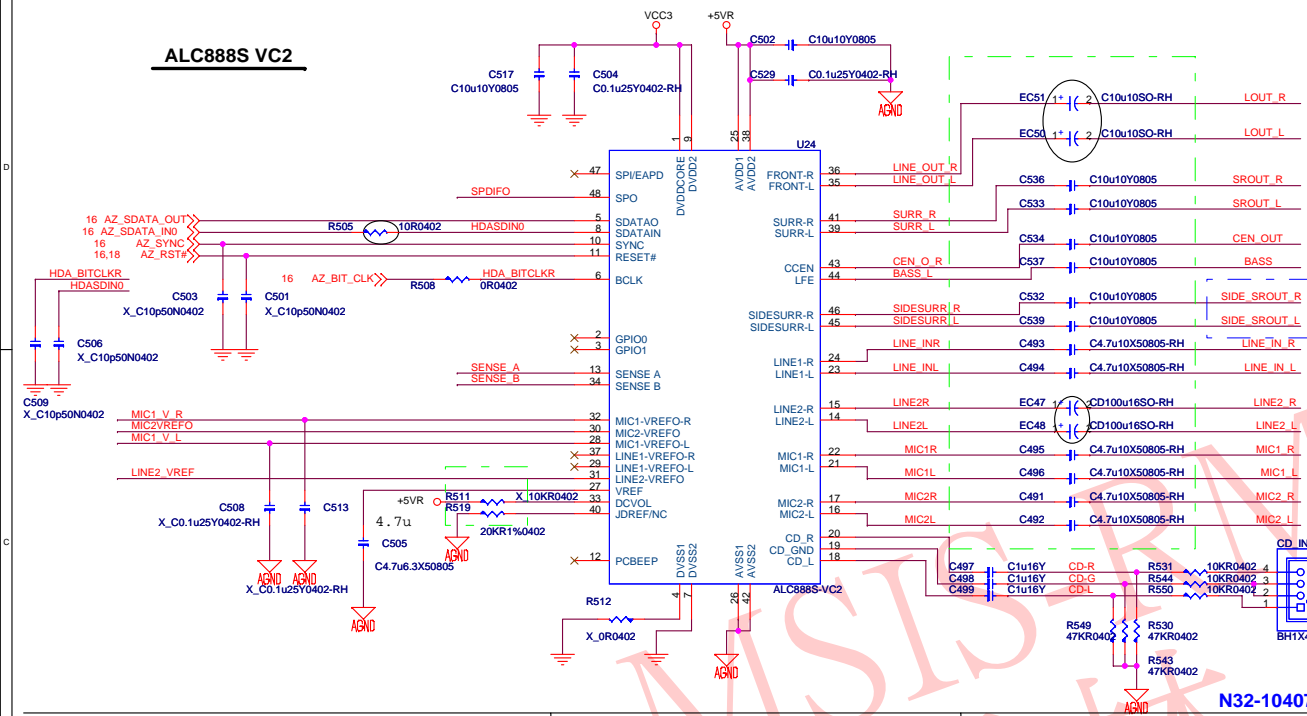


Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F0	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22		22	
	Green		Green

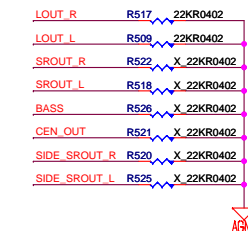
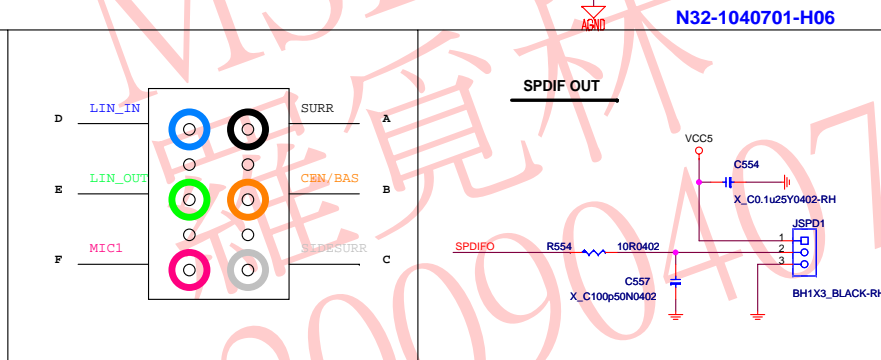
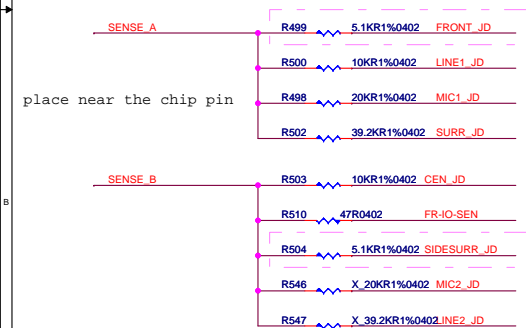
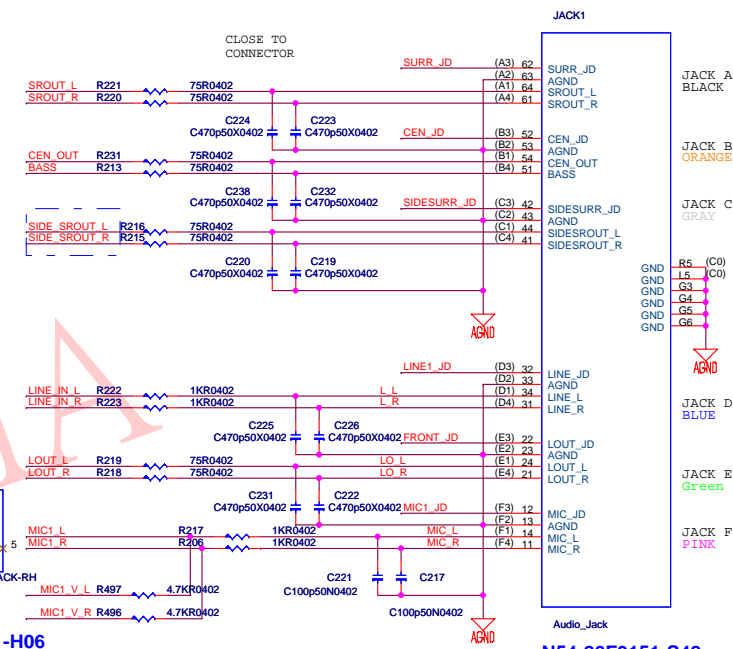


Micro Star Restricted Secret			
Title			Rev
LAN - Realtek 8111DL			0A
Document Number		MS-7599	
MICRO-STAR INT'L CO., LTD. No. 88, Li-De St, Jung-Huei City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, March 25, 2009 Sheet 22 of 36	

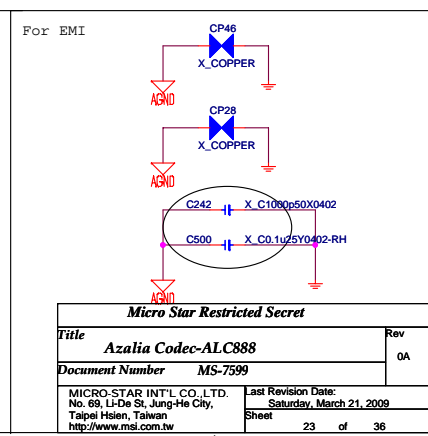
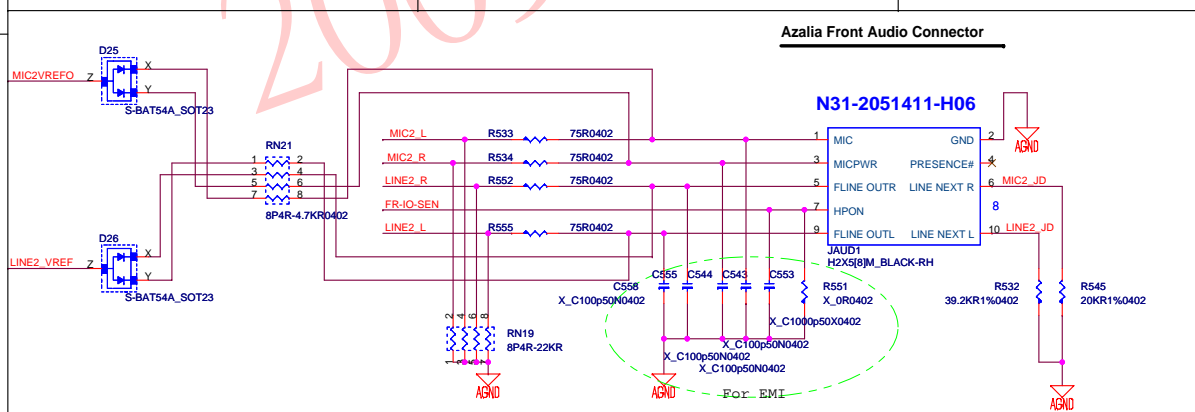
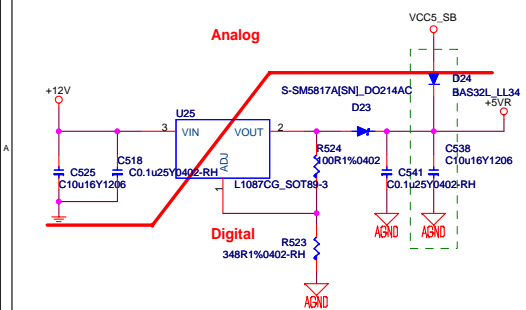
ALC888S VC2



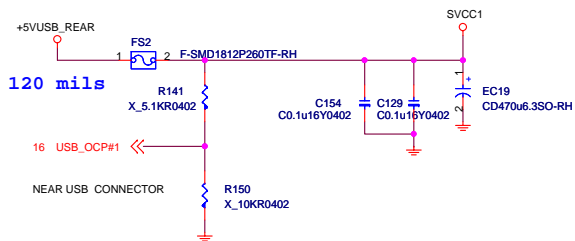
Rear audio jack



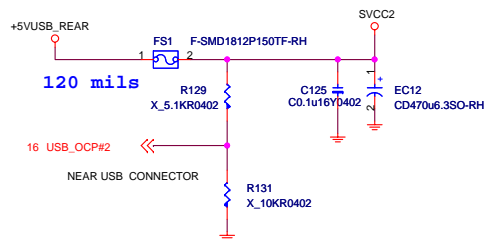
AUDIO CODE REGULATORS



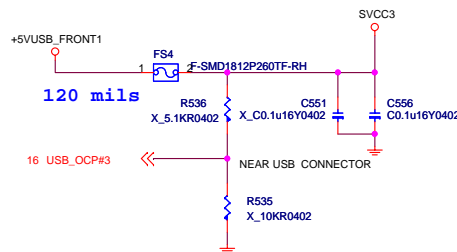
POWER CIRCUIT FOR USB PORT 0,1,2,3



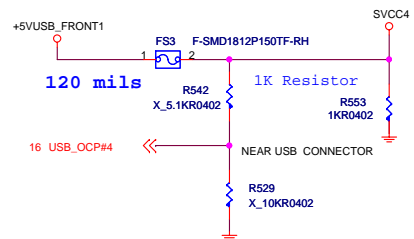
POWER CIRCUIT FOR USB PORT 4,5



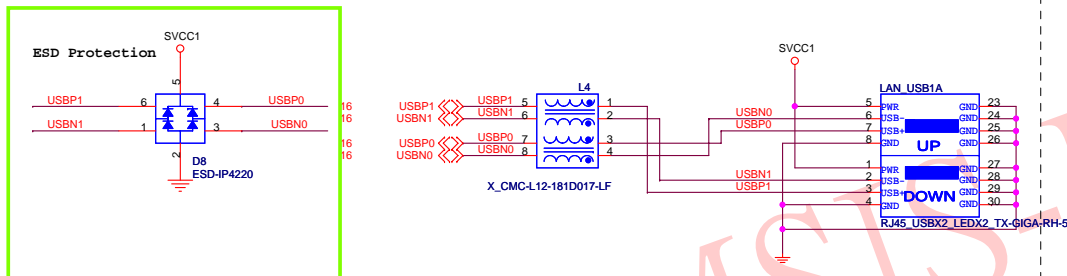
POWER CIRCUIT FOR USB PORT 6,7,8,9



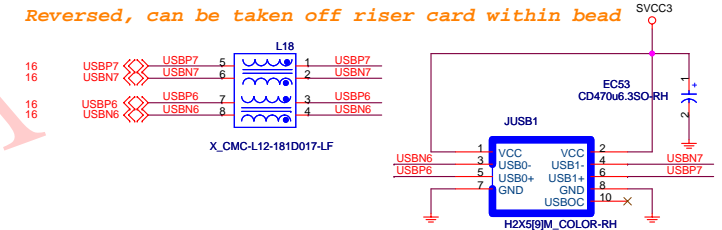
POWER CIRCUIT FOR USB PORT 10,11



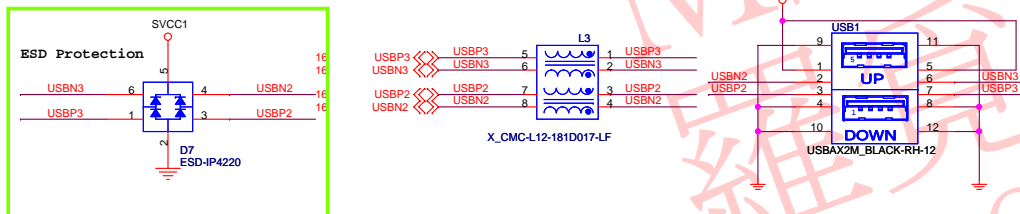
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



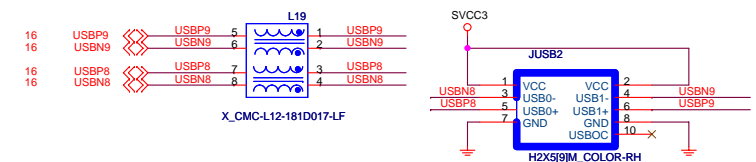
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



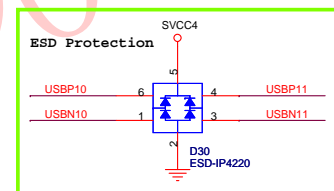
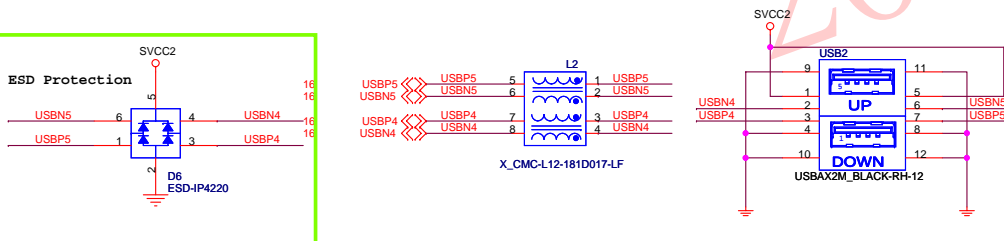
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



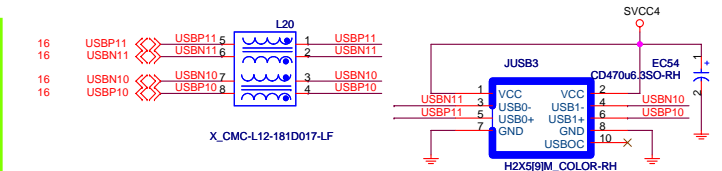
FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



REAR PANEL USB CONNECTOR FOR USB PORT 4,5

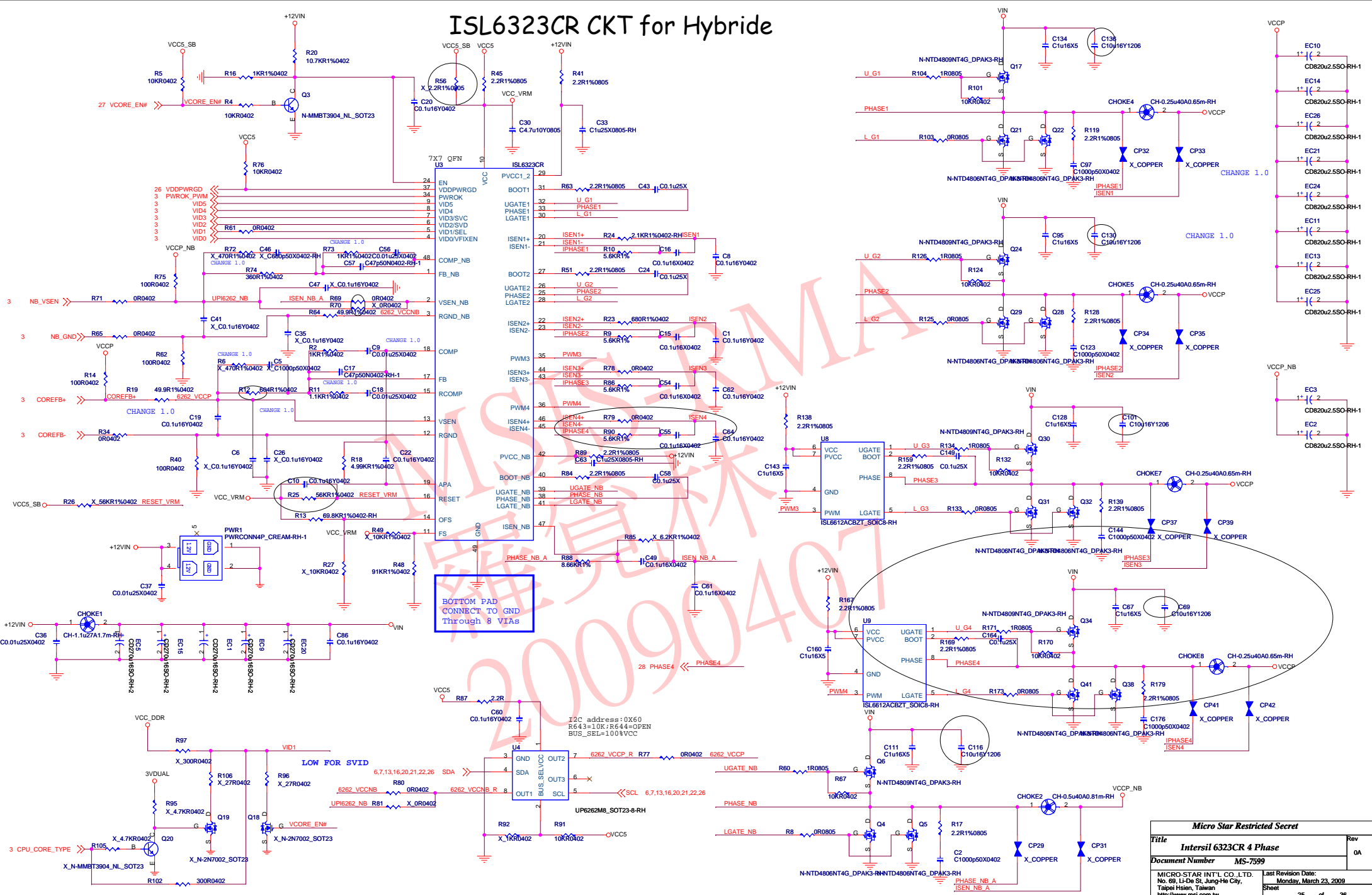


FRONT PANEL USB CONNECTOR FOR USB PORT 10,11

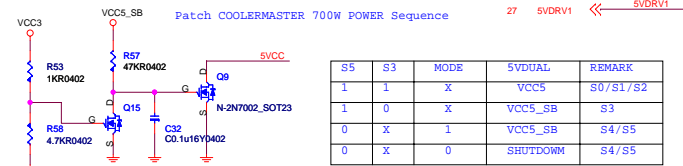
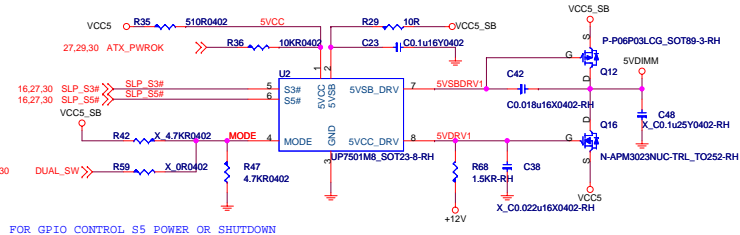


Micro Star Restricted Secret		
Title	USB CONNECTORS	Rev
Document Number	MS-7599	0A
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St., Jung-Ho City, Taipei Hsien, Taiwan		Last Revision Date: Thursday, March 26, 2009
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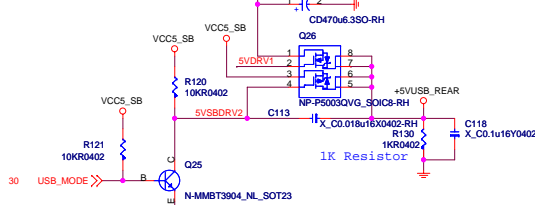
ISL6323CR CKT for Hybride



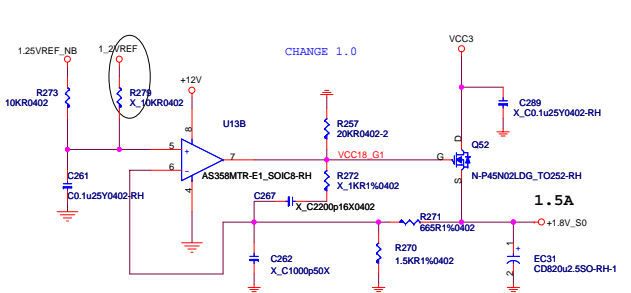
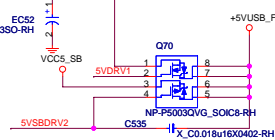
5VDIMM FOR DDR



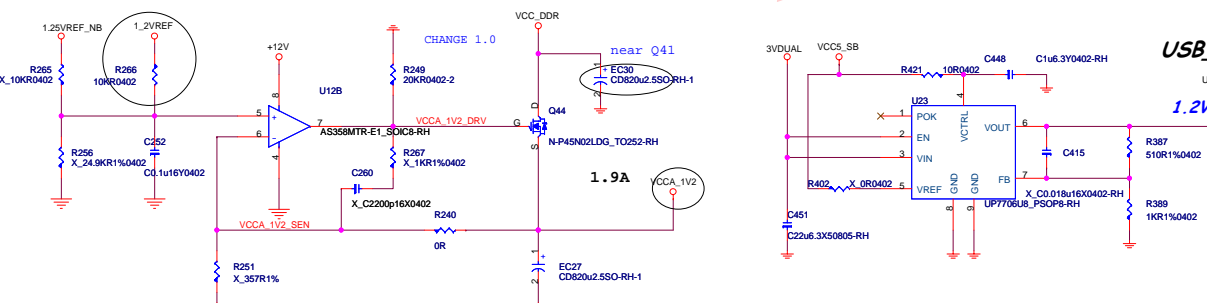
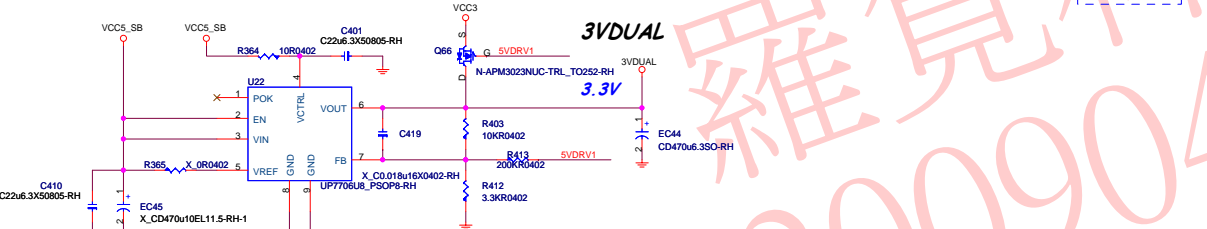
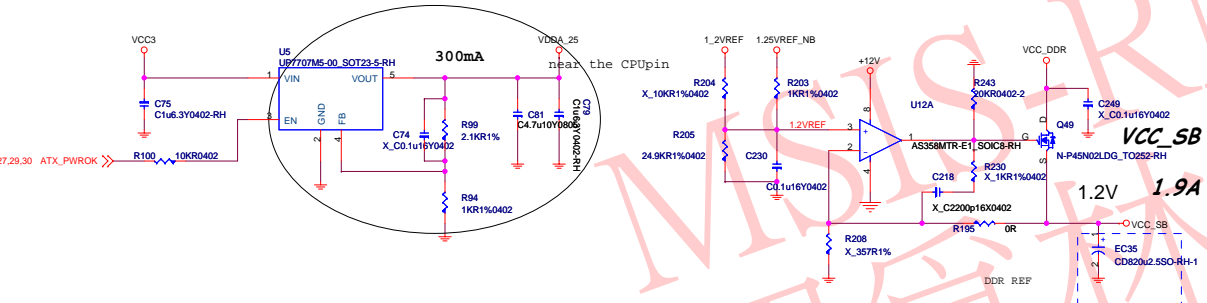
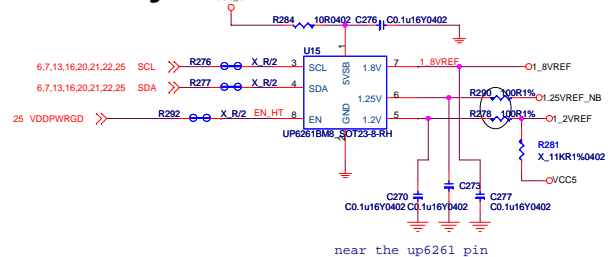
5VSB FOR Rear USB



5VSB FOR Front USB

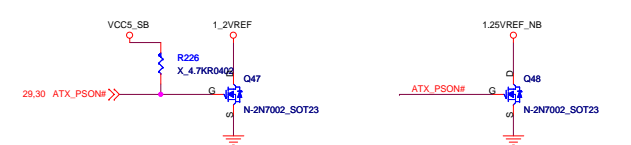
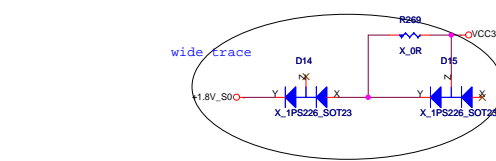
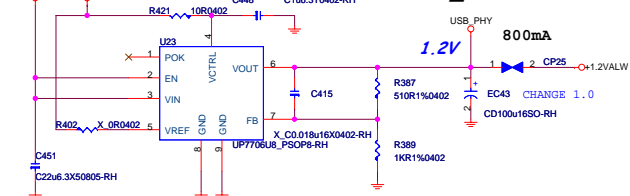


reference Voltage

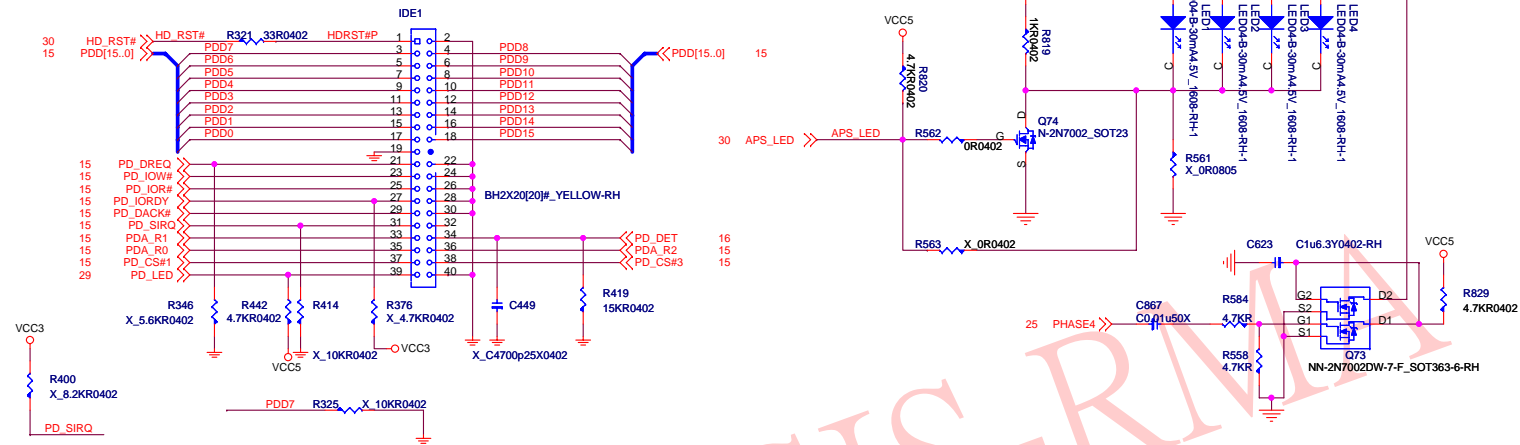


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USB_PHY



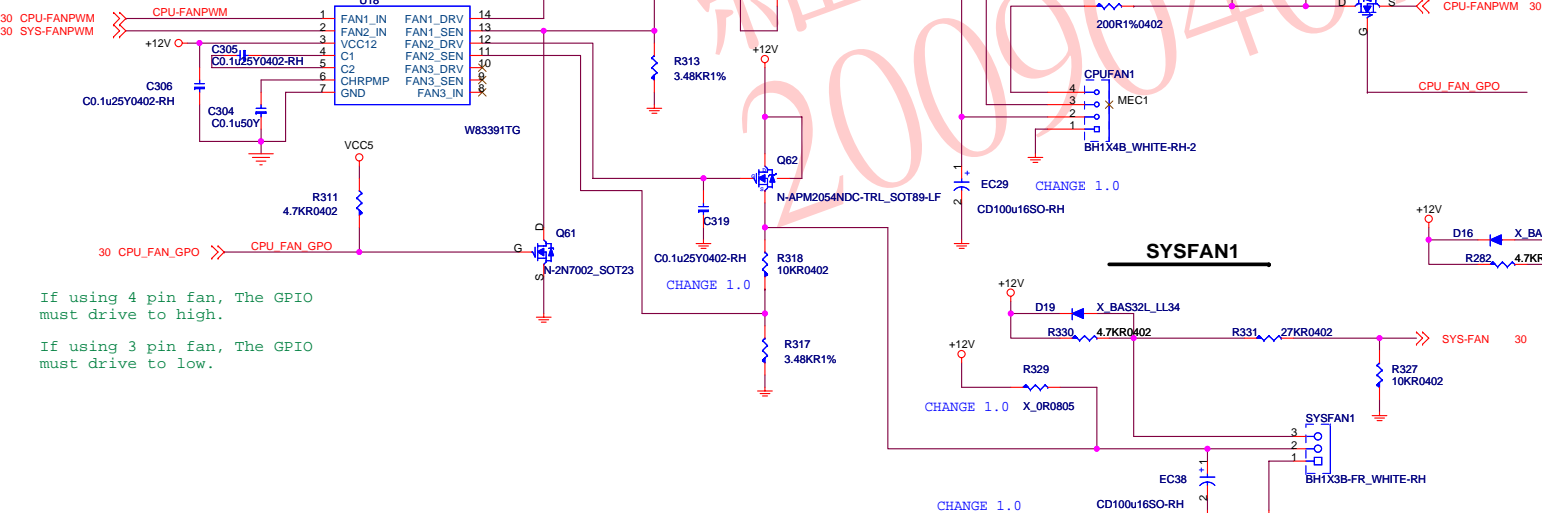
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Title	ACPI BY UPI	Rev
Document Number	MS-7599	0A
MICRO-STAR INT'L CO., LTD. No. 89, Lu-Ho St, Jung-Ho City, Taipei Hsien, Taiwan		Last Revision Date: Thursday, March 26, 2009
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FAN CONTROL

CPU FAN

CPU-FANPWM connect to 627EHF pin 115; default is PWM mode



If using 4 pin fan, The GPIO must drive to high.

If using 3 pin fan, The GPIO must drive to low.

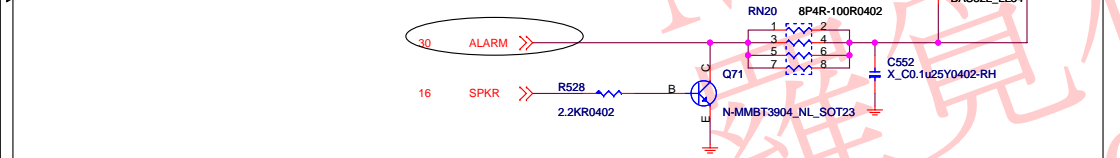
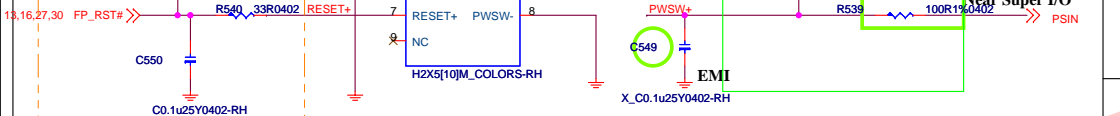
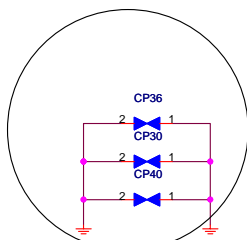
If using 3 pin fan, The Q54 will turn off to avoid the VCC5(R470) bias to CPU-FANPWM.

SYSFAN1

SYS FAN

Micro Star Restricted Secret	
Title	IDE Conn/FAN/LPT/SATA
Document Number	MS-7599
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, March 26, 2009 Sheet 28 of 36

Intel Front Panel

[illegible]

PS2 KEYBOARD & MOUSE CONNECTOR

SVCC2

RN1
8P4R-4.7KR0402

C21

R33
X_1KR1%0402

C0.1u25Y0402-RH

KB1

MS

KB

C34
C220p50N0402

C29
C220p50N0402

C28
C220p50N0402

C31
C220p50N0402

MINIDIN12P-RH

MSDATA

MSCLK

KBDATA

KBCLK

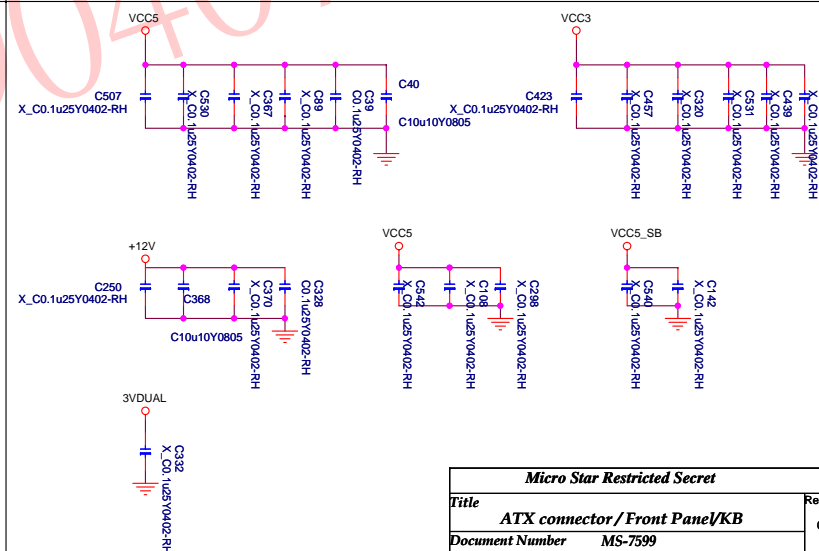
30

0

SERIAL PORT 1

The diagram shows the internal wiring of the SERIAL PORT 1. The microcontroller (GD75232_SSOP20) is connected to the BAS32L LL34 diode. The diode's anode (D4) is connected to +12VCOM, and its cathode (D5) is connected to -12VCOM. The microcontroller's pins are also connected to COM1 and DSUB-COMM_GREEN-RH-5.

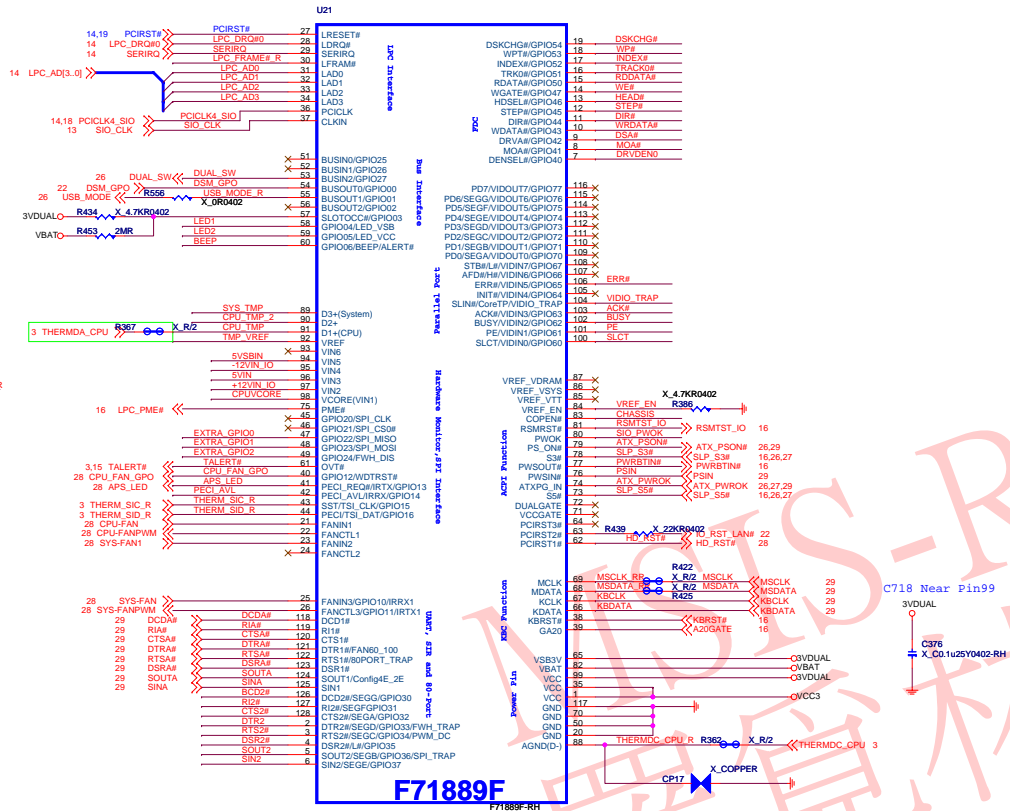
Microcontroller Pin	Signal	Value / Component
1	VDD	19
2	RA1	19
3	RA2	18
4	RA3	17
5	RA4	14
6	RA5	12
7	DA1	5
8	DA2	8
9	DA3	10
10	GND	VSS
11	RTSA#	16
12	DTRA#	15
13	SOUTA	13
14	RTSA#	16
15	DTRA#	15
16	SOUTA	13
17	RTSA#	16
18	DTRA#	15
19	SOUTA	13
20	RTSA#	16
21	DTRA#	15
22	SOUTA	13
23	RTSA#	16
24	DTRA#	15
25	SOUTA	13
26	RTSA#	16
27	DTRA#	15
28	SOUTA	13
29	RTSA#	16
30	DTRA#	15
31	SOUTA	13
32	RTSA#	16
33	DTRA#	15
34	SOUTA	13
35	RTSA#	16
36	DTRA#	15
37	SOUTA	13
38	RTSA#	16
39	DTRA#	15
40	SOUTA	13
41	RTSA#	16
42	DTRA#	15
43	SOUTA	13
44	RTSA#	16
45	DTRA#	15
46	SOUTA	13
47	RTSA#	16
48	DTRA#	15
49	SOUTA	13
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52	SOUTA	13
53	RTSA#	16
54	DTRA#	15
55	SOUTA	13
56	RTSA#	16
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59	RTSA#	16
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61	SOUTA	13
62	RTSA#	16
63	DTRA#	15
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88	SOUTA	13
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91	SOUTA	13
92	RTSA#	16
93	DTRA#	15
94	SOUTA	13
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96	DTRA#	15
97	SOUTA	13
98	RTSA#	16
99	DTRA#	15
100	SOUTA	13



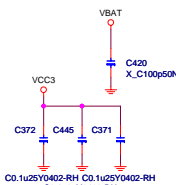
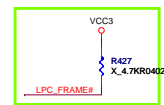
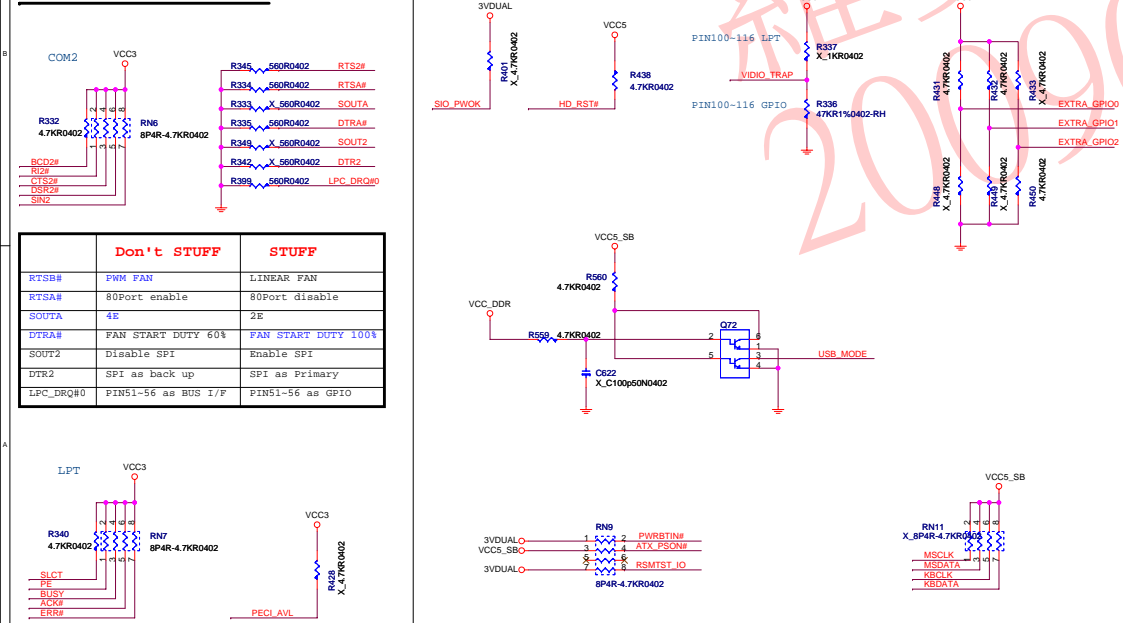
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Title	ATX connector / Front Panel/KB	Rev
Document Number	MS-7599	0A
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, March 25, 2009 Sheet 29 of 36

Super I/O

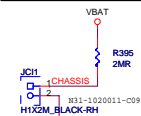
LPC SUPER I/O F71889



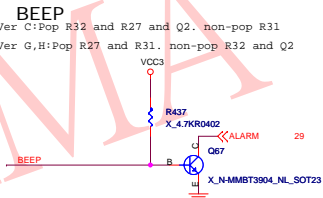
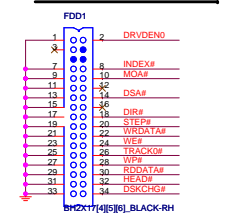
F71889 STRAPPING RESISTOR



Chassis Intrusion

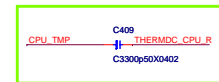


FLOPPY CONNECTOR

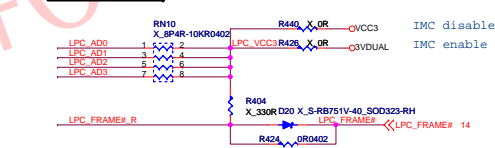


BEEP

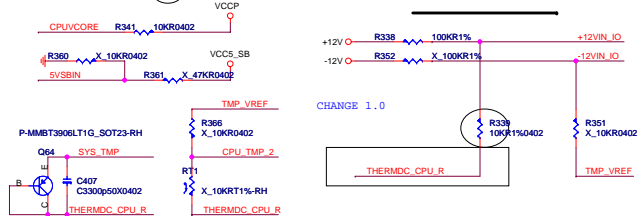
Ver C:Pop R32 and R27 and Q2. non-pop R31
Ver G,H:Pop R27 and R31. non-pop R32 and Q2



LPC PULL UP



Thermal Resistor



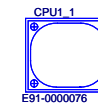
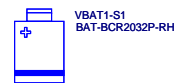
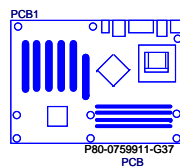
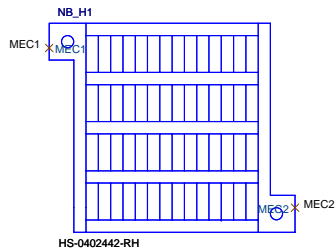
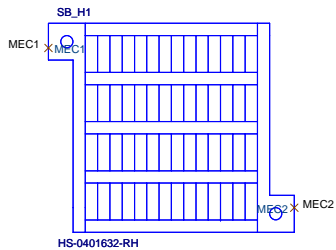
**NOTE: LOCATE CLOSE
STATUS PANEL**

Micro Star Restricted Secret

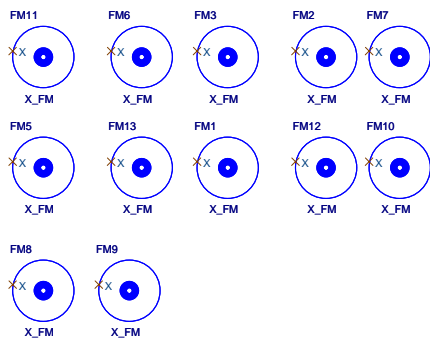
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Document Number		MS-7599
MICRO STAR INT'L CO. LTD.		Last Revision Date:

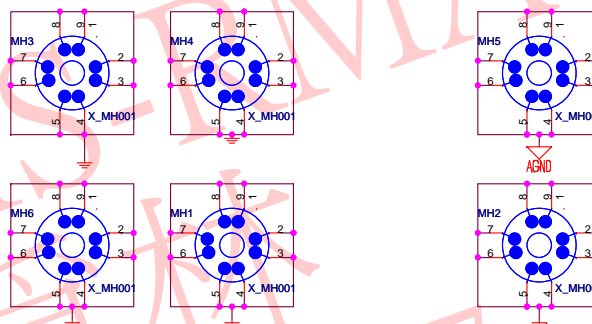
MICRO-STAR INT'L CO., LTD.
 No. 69, Li-De St, Jung-Hsi City,
 Taipei Hsien, Taiwan
<http://www.msi.com.tw>



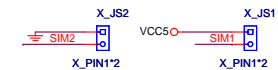
Optics Orientation Holes



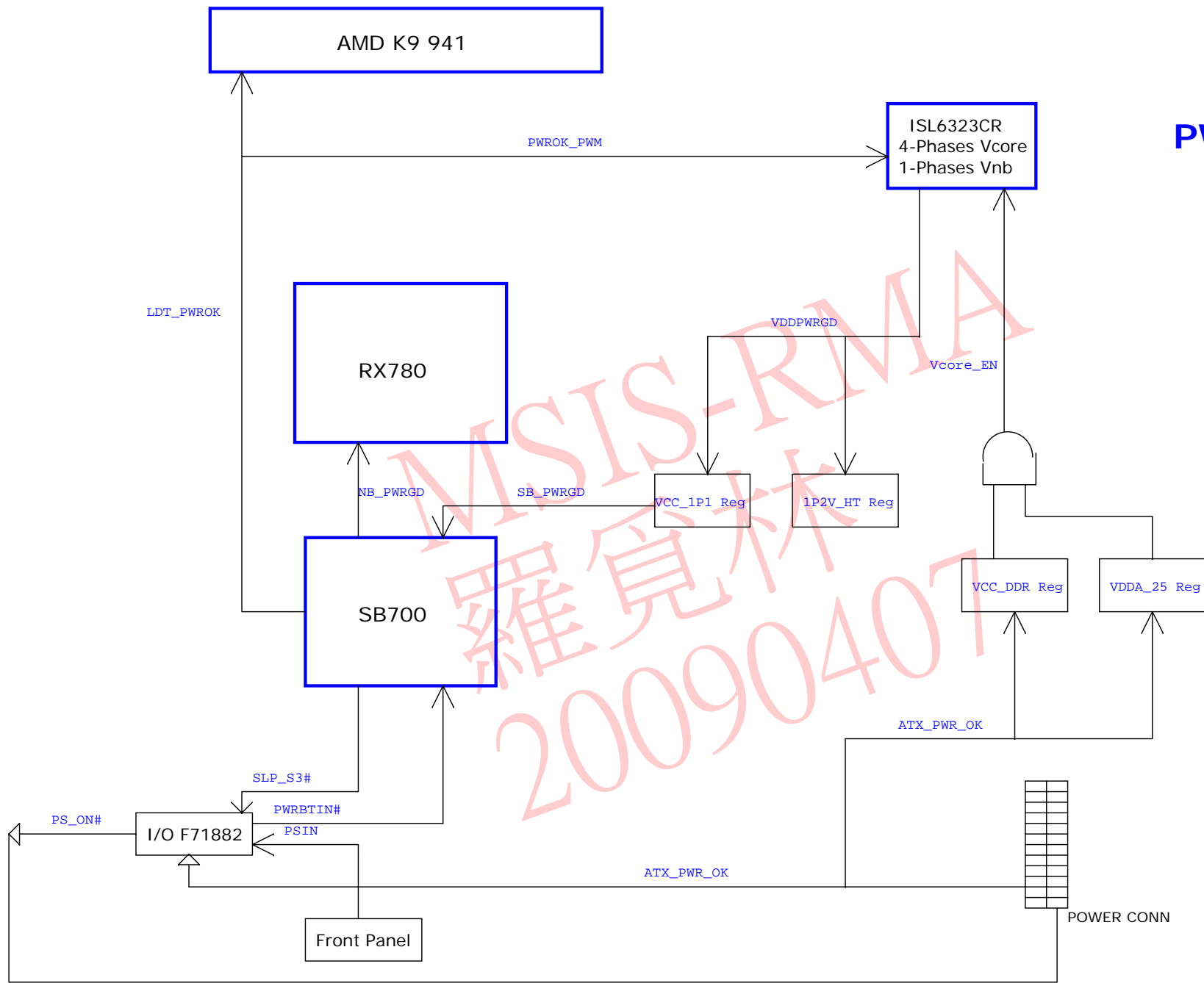
Mounting Holes



Simulation



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Title	MANUAL PARTS	Rev 0A
Document Number	MS-7599	
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PWROK MAP

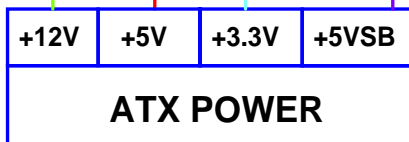
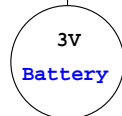
Micro Star Restricted Secret		
Title	PWROK MAP	Rev
Document Number	MS-7599	0A
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AM2R2			
VDD_CPU VDD_NB	-	110A	
0.8V - 1.55V Core	-		
VDDA 2.5V	-	0.2A	
VLDT 1.2V	-	0.5A	

RX780			
+1.1V CORE REGULATOR	-	8.7A	
+PCIE1.1V REGULATOR	-	2.5A	
+1.2V_HT REGULATOR	-	0.5A	
+PCIE1.8V REGULATOR	-	1A	

SB700			
+1.2V REGULATOR	-	758m A	
+3.3V DUAL	-	25m A	
1.2V DUAL	-	86mA	
+3.3V	-	86mA	
RTC(G3)	-	5uA	

FWH			
+3.3V (S0,S1)	-	107mA	



ISL6323			
VCCP	0.8375V-1.550V	125A	
	4+1 Phase Switch		
W83310DS			
VTT_DDR	0.9V	Linear	1.5A
Regulator			
VCC_2_5V		0.2A	

Regulator			
V_1P1_CORE	(S0,S1)		
	1.1V	Linear	3A
V_HT			
	1.2V	Linear	2.0A
+PCIE1.8V			
	1.8V	Linear	3A
5VDUAL1,2			
	5V	Linear	22mA
3VDUAL			
	3.3V	Linear	
PHY_VDUAL			
	1.2V	Linear	
UPI Regulator			
VCC_DDR	1.8V	Switch	20A
	Linear (S3)		425mA

DDR DIMM & TERMINATOR			
0.9V VTT_DDR	-	2A	
1.8V VCC_DDR (S0,S1)	-	10A	
1.8V VCC_DDR (S3)	-	400mA	

PCI Express x16 slot x2			
+12V	-	5.5 A	
+3.3Vaux (wake)	-	375mA	
+3.3Vaux (no wake)	-	20mA	
+3.3V	-	3.0A	

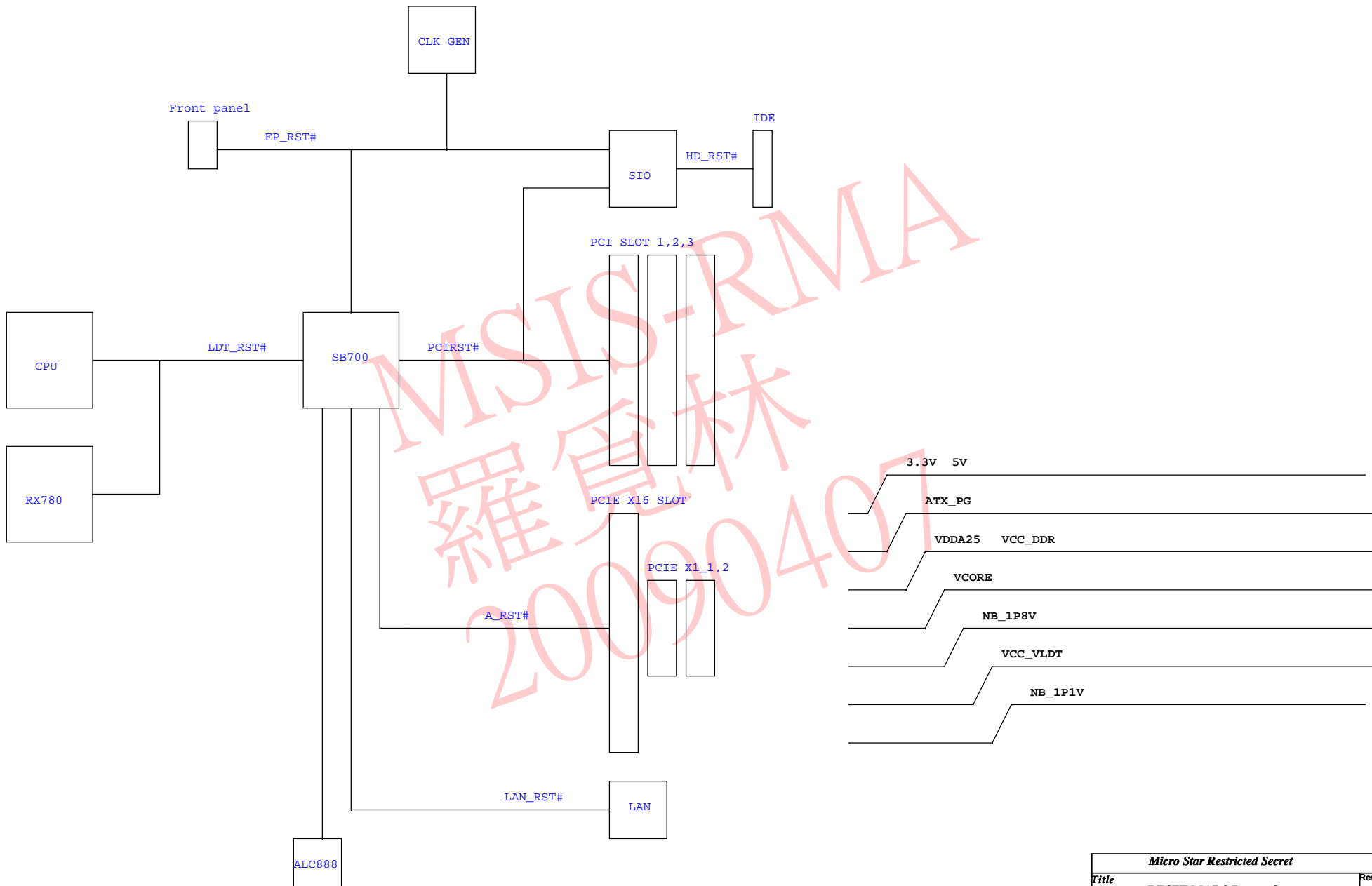
PCI Express x1 slot			
+12V	-	0.5 A	
+3.3Vaux (wake)	-	375mA	
+3.3Vaux (no wake)	-	20mA	
+3.3V	-	3.0A	

PCI slot x3			
+3.3Vaux (wake)	-	375mA	
+3.3Vaux (no wake)	-	20mA	
+3.3V	-	7.6A	
+5V	-	5.0A	
+12V	-	0.5A	

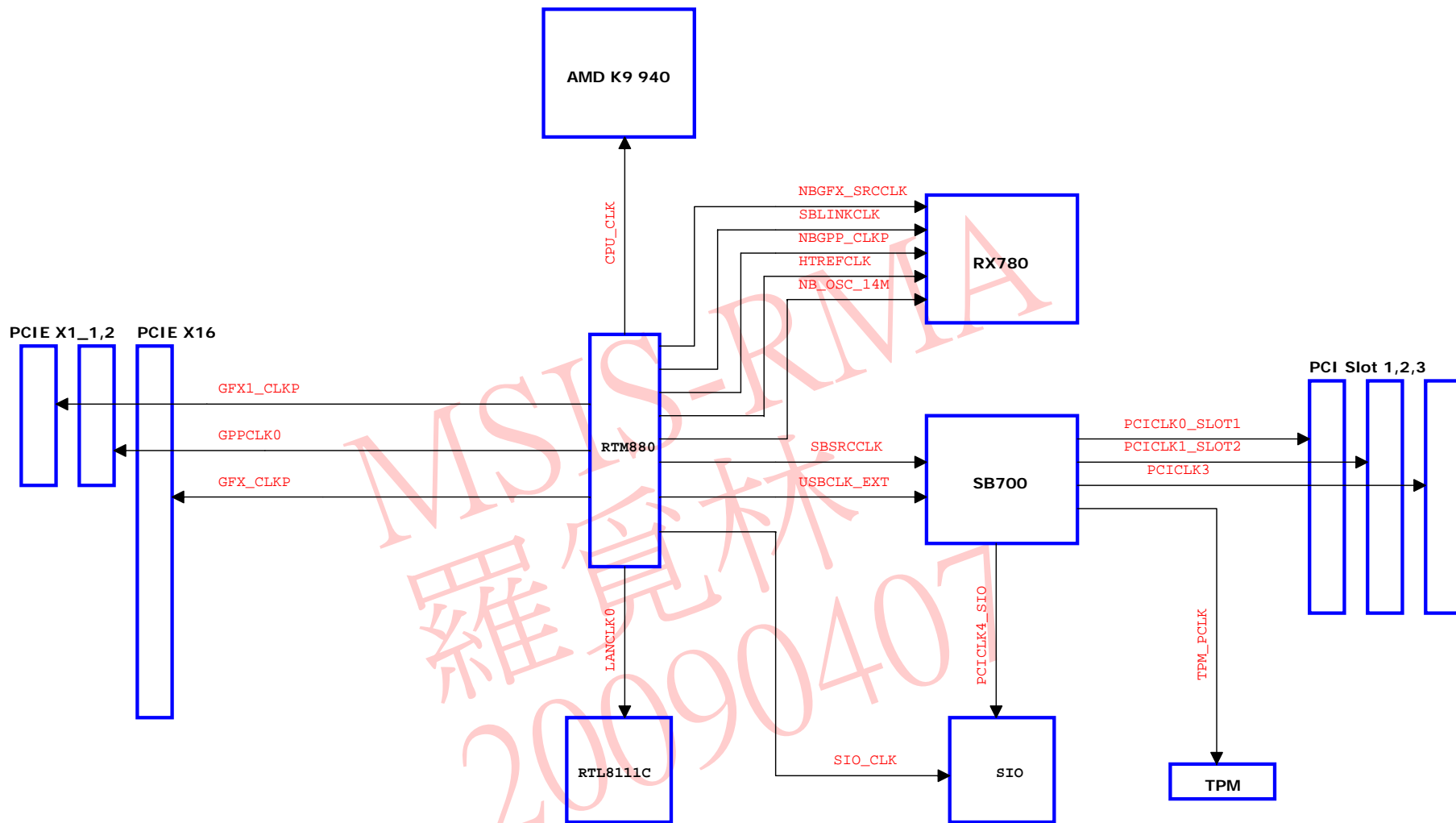
USB			
+5V (S0,S1)	-	4.0A	
+5V (S3)	-	20mA	

PS2			
+5V (S0,S1)	-	345mA	
+5V (S3)	-	2.0mA	

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1 add C66
2 change the C5,C6,C7,C12 ,C29,C30,C31,C32 footprint to 0805
3 add Q69
4 add EC53,EC56

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